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DESIGN AND IMPLEMENTATION OF HIGH SPEED AND ENERGY EFFICIENT 4 BIT 14 T CLA USING GDI TECHNIQUE

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Abstract- Carry look ahead adder (cla) is the important block in arithmetic logic unit due to its high speed of operation. In this paper we propose a high speed and energy efficient CLA using Gate Diffusion Input (GDI) Technique with 14 Transistor to reduce the area. The simplest way to design an adder is to implement gates to yield the required logic function. In this paper the entire work is done in LTSpice 180nm technology, Xilinx14.7 ISE tool. The resulting analysis shows that the proposed methods is better than conventional CMOS technology.

Keywords- Component; formatting; style; styling; insert (key words***).***

I. Introduction

Addition of binary bits in an important task among computational logic elements. There are some any ways of implementing the binary addition, encoding replication, static , CMOS dynamic logic, PTL (pass transistor logic) and adiabatic logic approach are the few logic technique to implement the same functional blocks. More power consumption leads to increase the temperature which influences the battery life in electronic device. In order to reduce the power consumption, area required and delays the number of transistors counts can be reduced in CLA. Addition is the basic operation of VLSI design. Ripple carry Adder(RCA) is the series connection of full adder in which carry propagate from first full adder to last one . in this process delay is more because output will not be generated until carry propagate to the lost full adder.
CLA is designed to overcome the problem in RCA

$$P_i = A_i + B_i$$
$$G_i = A_i.B_i$$
$$S_i = A_i + B_i + C_i$$
$$C_{i+1} = G_i + P_i.C_i$$

The scientist more started that for every 18 months the number of transistors integrated in the circuit would be doubled. MOSFET have explained removable scaling over the last four decades [1,2]. The increased performance would come from reduced transistor count [3], to meet the required amount of power and speed at various design abstraction levels have been subjected [4]. Different designs for adders have been proposed [5], [6]. The carry propagates and deviding adders in to two exact path are the to important technique proposed [7]-[10]. The digital circuits CLA which calculate sum and produce the output after each and every full adder circuit.

$SUM = A\,xor\,B\,xor\,C_{in}$, from the expression $A\,xor\,B$ used in carry

$$C_{out} = G_i\,or\left(P\,and\,C_{in}\right)$$
$$G_i = A\,xor\,B$$

$P_i = A\,xor\,B$ in this way the total delay of the circuit is reduced in CLA

$C_i = 0$ Then

$$C_1 = 0 + 0.0 = 0$$
$$C_2 = 0 + 0.0 = 0$$
$$C_3 = 0 + 1.0 = 0$$
$$C_4 = 0 + 1.0 = 0$$

To reduce the area of CLA here we proposed a novel method of designing CLA is GDI technique.
The main aim of the paper is to design and implement of low power and high speed 8 bit CLA using static CMOS logic and GDI technique. The design is performed in 180nm technology.

II. GDI(Gate Diffusion Input) Technique

Low power combinational circuit design is explained by a novel gate diffusion input technique. The technique reduce the power , delay and area of the design.
The basic GDI cell contains three terminals which are G (Gate), N(one of the input to source/ drain of nMOS) and P(input to source/drain of pMOS) as shown in figure 1.
The functions tabulated in the table -1 are more, complex in CMOS technology, but in GDI each function implemented with only two transistors.

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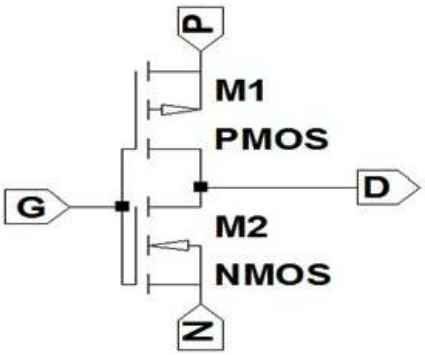

Figure.1. Basic GDI Cell

Table.1. Functionality of GDI

N	P	D	G	Function
0	B	A	$\overline{A}B$	F1
B	1	A	$\overline{A}+B$	F2
1	B	A	$A+B$	OR
B	0	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
0	1	A	A	NOT

III. Existed Circuit

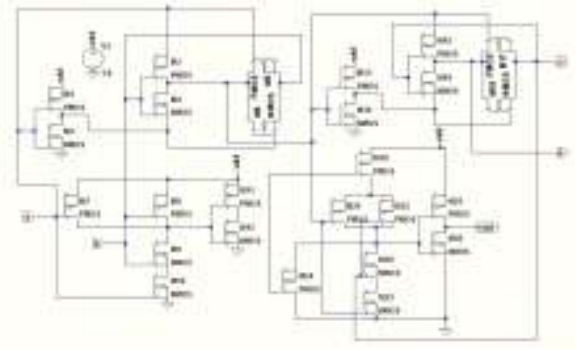

Figure.2. SINGLE BIT CMOS CLA

The number of transistors are used to design a single bit CMOS CLA(carry look a head adder) is 26 as shown in figure 2. It is a part of CLA to design 16 bit cla. The total number of transistors used for the design of existed CMOS CLA is 104.

IV. Proposed GDI 4-CLA

Figure 3 of CLA block explains about how the carry propagate from stage one of adder one to last stage of the adder.

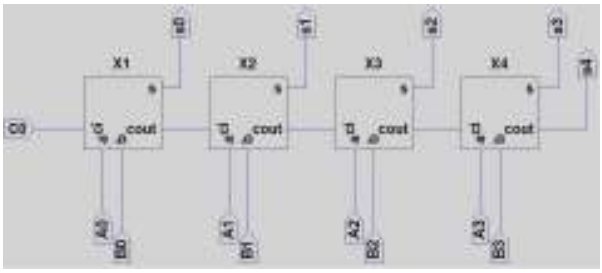

Figure.3. Block Diagram of 4-bit CLA

This carry propagation among the adders was explained in CMOS CLA , but the hardware required to design a 4-bit CLA is redused using GDI Technique.

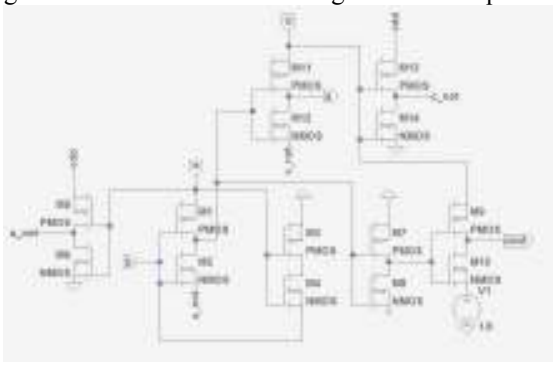

Figure.4. SINGLE BIT GDI CLA

The figure 4 demonstrates that the CLA increases the speed by reducing the amount of delay required to determine the carry bits. The operation of CLA depends on two things , calculates position of each bit, whether that position will propagate a carry of one comes in from the right. The second one is to combine these calculated values.

The above Figure.4 represents the proposed circuit designed by carry GDI technique primary design of XOR block has 4 transistor and gate designing utilized 4 transistor and the function g+p.Cin utilized 4 transistor and the overall 1 bit CLA is block designed using only 14 transistor in GDI technique. If a=0, b=1, Cin=0 then M1 will be in the OFF state and M2 will be in the ON state then the output will be (O1) 1 further M5 will be in the ON state and M6 will be in the OFF state then the output of M5 and M6 is (a_not) 1.with the inputs of a,b,Cin of above values M3 is ON and M2 is OFF and the output from M3 is (O2) 0, This output of M3 is used for power supply for M9.According to the inputs M15 is OFF and M16 is ON then the output is (S)1, and M17 is ON and M18 is OFF then the output is(C_not) 1 Now the M7 is ON state and M8 is OFF state and the output is (O3) 0 and M9 is ON ,M10 is OFF then Cout is 0

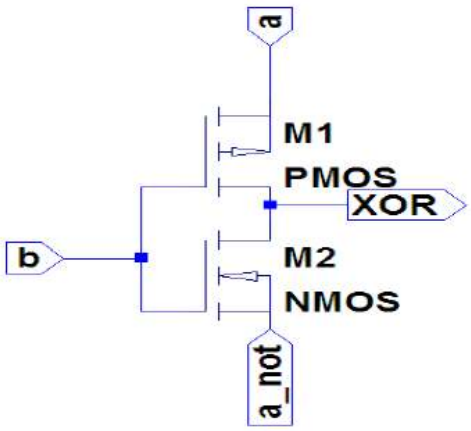

Figure.5. XOR GDI circuit

The above Figure 5 has two M1 and M2 transistors with *a* and *b* as inputs, if the input *a* and *b* are at logic low level then M1 gets into ON state and M2 goes to OFF state and produces logic low as the output. If *a* is at logic high and *b* is at logic low then M1 gets into ON state and M2 goes to OFF state and produces the logic 1 as the output, similarly *a* is at low and *b* is at high then M1 remains in OFF state and M2 goes to ON state and produces the logic high as the output. If both *a* and *b* are at logic high state M1 remains in OFF state and M2 goes to ON state and produces the logic low as the output.

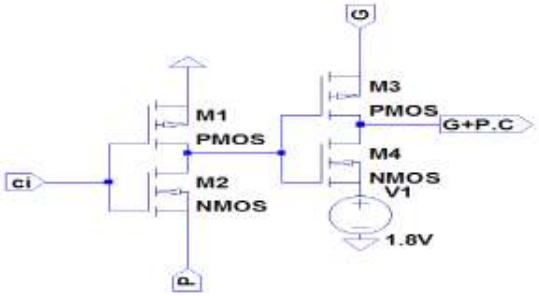

Figure.6. AND-OR GDI circuit

Fig-6 shows AND-OR gate functionality of G and S are at high as well as cin is low, then M1 is in ON state , M2 will be OFF state, M3 is in ON state but M4 is in OFF state, there fore output goes to high.

V. Result Analysis And Comparison

Table.2. represents that the proposed circuit gives improvement in area, power and delay analysis in contrast to other conventional technique. The area consideration shows that the transistor count of proposed work is greatly reduced compared to conventional CMOS technique, As transistor count reduces, hardware complexity of the circuit decreases, delay decreases leading to decrease in power consumption. Figure.10. shows the timing delay and power analysis which is tabulated in table 2. In our proposed work power reduced by 36%, area reduced by 47%, time delay decreased by 67% compare to conventional CMOS technique. Time delay is calculated by using LTspice, area and power is calculated by using Xilinx 14.7 ISE tool by implementing on Basys-3 Artix7 devices.

Table.2. Comparison Table

	Area (transistor count)	Time delay(sec.)	Power (mW)
CMOS	104	124ps	29.12
GDI	56	3.5ps	19.27

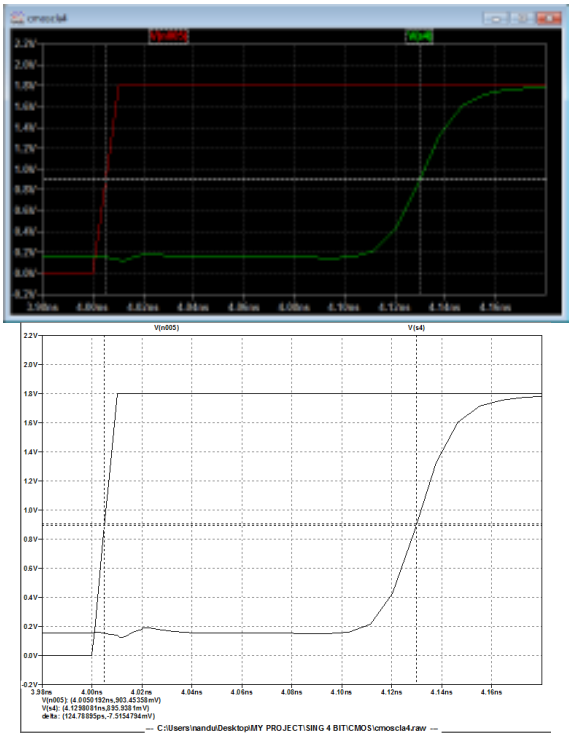

Figure.7- Bit CLA output analysis in CMOS LOGIC

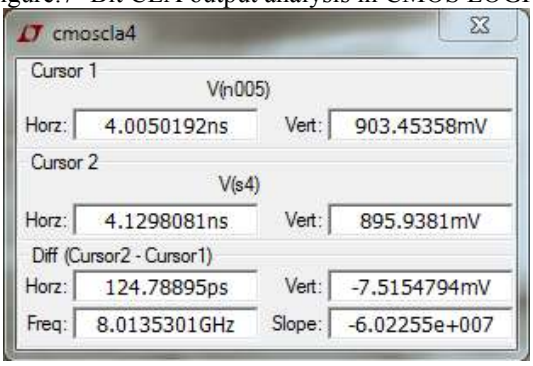

Figure 8- Bit CLA Time delay analysis in CMOS LOGIC

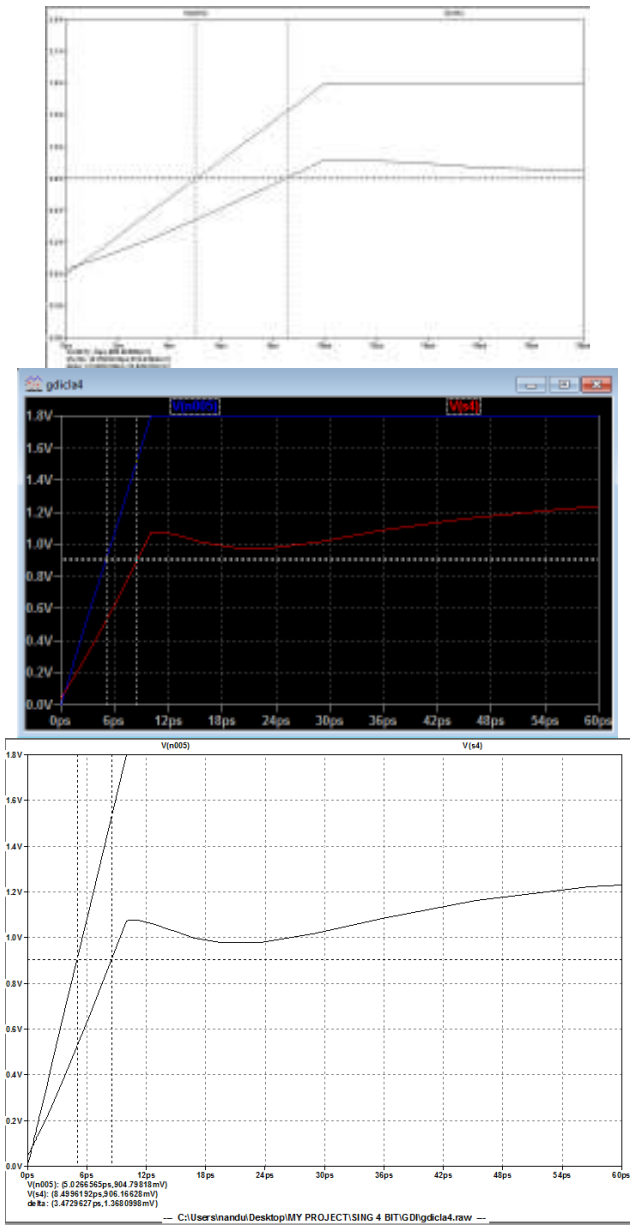

Figure 9-Bit CLA output analysis in GDI Technique

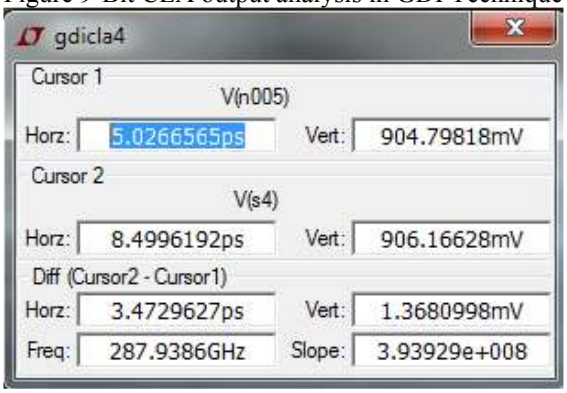

Figure 10-Bit CLA Time delay analysis in GDI Technique

VI. Conclusion

From the above analysis it can be concluded that our proposed 4-bit GDI CLA circuit has showed signs of improvement execution in case of area, delay and power comparatively with conventional 4-bit CMOS CLA. It shows that GDI approach of CLA design is better for complex data processing application.

References

[1]. M. I. Elmasry, ―Digital MOS integrated circuits: A tutorial;' DigitalMOS Integrated Circuits. New York: IEEE Press pp. 4-27.

[2]. A. Kapuma,‖ CMOS circuit optimization,‖ Solid-State Electronics, vol. 26, no. 1, pp: 47-58, 1983.

[3]. B. K. Mohanty and S. K. Patel, "Area–Delay–Power Efficient Carry-Select Adder," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 61, no. 6, pp. 418-422, June 2014.

[4]. B. Shao and P. Li, "Array-Based Approximate Arithmetic Computing: A General Model and Applications to Multiplier and Squarer Design," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 4, pp.1081-1090, April 2015.

[5]. M. S. Khairy, A. Khajeh, A. M. Eltawil and F. J. Kurdahi, "Equi-Noise: A Statistical Model That Combines Embedded Memory Failures and Channel Noise," IEEE Transactions on Circuits and Systems I: Regular Papers, vol.61, no. 2, pp. 407-419, Feb. 2014.

[6]. R. Ye, T. Wang, F. Yuan, R. Kumar and Q. Xu, "On reconfiguration oriented approximate adder design and its application," Proceedings of IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2013, pp. 48-54.

[7]. H.R. Mahdiani, A. Ahmadi, S.M. Fakhraie and C. Lucas, "Bio-InspiredImprecise Computational Blocks for Efficient VLSI Implementation of Soft-Computing Applications," IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 57, no. 4, pp. 850-862, April 2010.

[8]. D. Shin and S.K. Gupta, "A Re-design Technique for Datapath Modules in Error Tolerant Applications," Proceedings of 17th Asian Test Symposium(ATS), 2008, pp. 431-437.

[9]. N. Zhu et al. "Design of Low-Power High-Speed Truncation-Error-Tolerant Adder and Its Application in Digital Signal Processing," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 18, no. 8, pp. 1225-1229, Aug. 2010.

[10] N. Zhu, W.L. Goh and K.S. Yeo, "An enhanced low-power high-speed Adder for Error-Tolerant application," Proceedings of International Symposium on Integrated Circuits (ISIC), 2009, pp. 69-72.