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ANALYSIS OF LOW POWER FULLADDER USING TRANSISTORS

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Abstract-The paper proposes the novel design of a 3T EX-NOR gate combining complementary CMOS and multiplexer. This paper presents as low power efficient full adder with transistors(T).All the DSP processors consists of adder circuits .The power consumption in a full ladder circuit is majorly due to EX-NOR gates. Adders have become one of the important components in the digital world in such a way that there is no design without it .Adders are not only used for additions ,but also used in many other functions like Subtractions, Multipliers, and Dividers etc .In the field of Very Large Scale Integration(VLSI), Adders are used as the basic component from processors to ASIC's. Hence a well optimized Adder design is needed .A single bit full adder using transistors has been designed using proposed XNOR cell, which showspowerdissipationof581.542µW. Simulations have been performed by using MICROWIND tool.

Keywords- Low power, Ex-Nor gate, full adder less delay

I. Introduction

With exponential growth of portable electronic devices like laptops, multimedia and cellular device, research efforts in the field of low power VLSI (very large-scale integration) systems saved increased many folds. With the rise in chip density, power consumption of VLSI systems is also increasing and this further, add store liability and packaging problems. Packaging and cooling cost of VLSI systems also goes up with high power dissipation. Now a day's low power consumption along with minimum delay and area requirements is one of important design consideration for IC designers. There are three major source of power consumption in CMOSVLSI circuits:1) switching power duet charging and discharging of capacitances,2)short-circuit power due to current flow from power supply to ground with simultaneous functioning of p-network and n-networks, 3) static power due to leakage currents. Binary addition is basic and most frequently used arithmetic operation in microprocessors, digital signal processors (DSP) and application-specific integrated circuits (ASIC) etc. Therefore, binary adders are crucial building blocks in VLS circuits and efficient implementation of these adders affects the performance of entire system. In recent years various types of adder using different logic styles have been proposed [1-12]. Standard CMOS 28transistor adder using pull up and pull- down network with14 NMOS transistors and 14 PMOS transistors is most widely reported 1].In[2] a 16 transistors full adder cell with XOR/XNOR, pass transistor logic(PTL)and transmission gate is reported. Complementary pass-transistor logic (CPL) with32transistor saving high power dissipation and better driving capability Is reported in [4].Transmission gate CMOS adder (TGA) based on transmission gates using 20transistors is reported in [5]. Main disadvantage of TGA is that it requires double transistors count that of pass transistor logic for implementations of same logic function. A transmission function full adder (TFA) based on transmission function theory used 16 transistors [6]. Multiplexer based adder (MBA) having 12 transistors and elimination of direct path to power supply is reported in [7]. Static energy recovery full(SERF) adder using 10transistorswith reduced power consumption at the cost of higher delay is presented in [8].Another design of full adder with 10 transistors using OR/XNOR gates is also reported in [9].A hybrid CMOS logic style adder with 22 transistors is reported [10]. In [11]a full adder circuit using22transistors based on hybrid pass logic (HPSC)is presented.. Full adder for applications using three inputs XOR is also reported in 12]. The function of full ladder is based on following equation ,given three single bit inputs as A,B,C in and it generates two outputs of single bit Sum and Count, where:

Sum = (A xor B) x o rCin (1)

Count= A.B+ Cin (A xor B) (2)

Structured approach for implementation of single bit full adder using XOR/XNOR has been reported [3] as showninFigure1.Withdecomposition of full adder cell in to smaller cells, equations (1) and equations (2) can be rewritten as

Sum= H XOR Cin= H .Cin'+H' Cin(3)

Count=A.H'+ Cin .H (4)

Where H is half sum (A XOR B) and H' is

Complement on.

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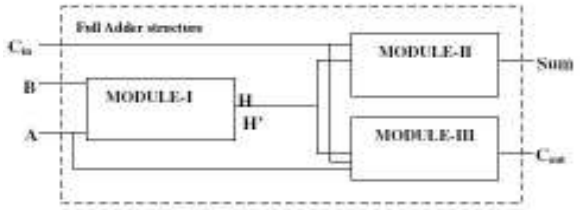

Figure 1: Structure Of Single Bit Full Adder

The exclusive–OR (XOR) and exclusive–NOR (XNOR) gates are the basic building blocks of a full adder circuit. The XOR/XNOR gates can be implemented using ANDOR ,and NOT gates with high redundancy[1].Optimized design of these gates enhances the performance of VLSI systems as these gates are utilized as sub blocks in larger circuits. XNOR/XOR design with less number of transistors, lesser power dissipation and delay are highly desirable for efficient implementation of the large VLSI system .XOR gate based on eight transistors and six transistors have been used in many earlier designs [1, 13]. Four transistors PTL based XOR gates with limited driving capabilities have been reported in[14].Different designs for XOR and XNOR gates using four transistors have been presented in[9,15-16]. Design for three inputs XOR gate instead oftwoinputs.XOR/XNOR design with ten transistors based on transmission gates XOR/XNOR circuits with dual feedback rectification of degraded logic problem Different power efficient adder designed with body biasing single techniques

The rest of paper is organized as follows: In Section II,a new three transistors XNOR gate has been reported and single bit full adder circuit based on XNOR gates and multiplexer has been designed. In section III results o f proposed XNOR cell and single bit full adder designed in previous section have been presented and compared with previous reported circuits .Section IV concludes the work.

II. System Description

Proposed design of XNOR with three transistors has been shown inFigure2.In XNOR circuit, the gate lengths of all there transistors have been taken as 0.35µm. Width (Wn) of NMOS transistors N1 and N2 has been taken 5.0µm and 1.0µm respectively. Width (Wp) for transistor P1 has been taken as 2.0µm.In proposed XNOR, when A=B=0 output is high because transistor P1isonandN1,N2transistors are off .Within put combinations of A=0andB=1circuit shows low output as transistor P1is of f and output node is discharged by transistor N2,which is in on condition. In case when A=B=1, output node shows high logic as transistor N1 is on and high logic Is passed to output .Width (Wn) of N1 is made large to provide low resistance and due to which signal B is passed to output with less delay, whereas P1gives higher resistance and higher delay topass the Vdd signal.For N1 transistorwidth has been increased which provides reduction in threshold voltage as shown in equation(5).Due to this decrease in Vt the degradation in the output logic is reduced and signal shows sufficient voltage swing. It is obvious that by increasing the W it is possible to reduce the voltage degradation .Further, duet higher delay provided by PMOS transistor (P1), drain source voltage (Vds) of N1 is increased gradually.Transistor N1 operates in non-saturation region and then goes to saturation region. On resistance of MOS transistor consists of the series combination of Rd (drain resistance) and Rs (source resistance) and channel resistance .As for superior switching action higher Vgs is desirable. Transistor N1 has larger width, less resistance and higher Vgs so switching is very fast in this case. WhenVds is less than Vgs-Vt but greater than zero the channel resistance in non saturation region is given as by

$$Ron=L/(Vgs-Vt-Vds) \quad (5)$$

Here,Ron is reduced and signal Bi s rapidly passed.

To output which further increase the Vds of transistor N1.Insaturation region output resistance Ron varies with ih Vds .As Vds is increased the pinch off moves towards our ce region and there Is incremental change in output impedance .Output resistance is given as

$$(2L/(1-\Delta L/L))1/Id\sqrt{qNb/2\epsilon si}(Vds-Vds'sat) \quad (6)$$

Where L is the channel length, _L is the small change in length due to increased Vds, Id is the drain current, and Nb is doping concentration. With higher Vds, the output resistance increase in saturation region. This condition is applicable for both N1 and N2 because of high Vds for these transistors. Due to higher resistance provided by N1 and N2 in saturation region the high output logic is maintained at output node. In another case when A=1 and B=0 both transistors (P1 & N1) are on and output node is is charged rapidly by N1 and N2 transistors. In this case with A=1 transistor N1 turns on which further turn on the transistor N2 and a conducting path is provided by N1 and N2. This connectivity of output node with ground discharges the output node. The switching speed of N1is higher than N2 because delay is inversely proportional to channel width [1]. Due to on condition of transistor N1 the gate voltage of N2 increase above its threshold voltage and transistor N2 also goes in on condition. In this position the circuit is just behaving like an inverter with A=1 as input and gives output as low logic. Transistor P1 is just acting as load resistance with grounded gate input (B= 0) .XOR operation can be obtained with addition of additional inverter. Signals levels are also restored to Vdd in the proposed design by addition of inverter with little increase in power consumption. Complete XNOR/XOR module with five transistors has been shown in Figure 2.Typical values of transistor widths (Wp=2.0µm) for P2 and (Wn =1.0µm) for N3 have been taken for inverter section. Simulations of XNOR

gate and XNOR/XOR cell also have been carried out with varying supply voltage from [3.3-1.8] V gate

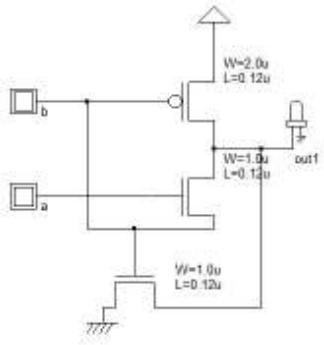

Figure2: Design Of proposed three transistor E xor Configuration

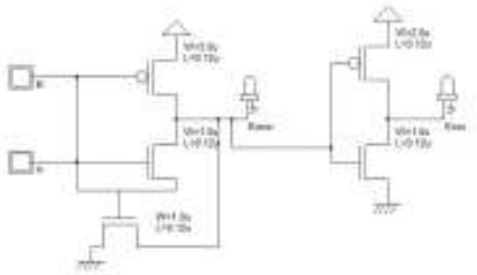

Figure3: Design Of Exnor- Exor Configuration

Full ladder circuit can be implemented with different combinations of XOR/XNOR modules and two multiplexer [2, 16] but this approach has not been used in current work as proposed XNOR/XOR cell shows high power consumption than single XNOR gate. Proposed full adder circuit has been implemented by two XNOR gates and one multiplexer block as shown in block diagram of Figure4 (a).Sum Is generated by two XNOR gates and Count is generated by multiplexer block. The single bit full adder using proposed XNOR gate with eight transistors has been implemented andshowninFigure4(b).For multiplexer section typical values of width (Wn &WP)1.0µm&2µm for NMOS and PMOS transistors have been taken with gate length of0.35µm. Simulations have been performed usingmicrowindbasedonTSMC0.35µm CMOS technology with supplyvoltageof3.3V

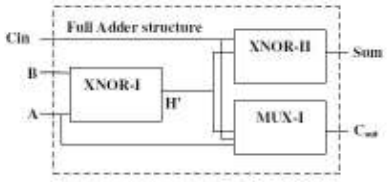

Figure4: Full Adder Using Two XNOR Gates And Multiplexer Block Diagram

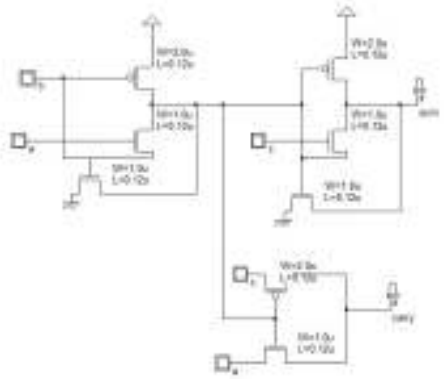

Figure5: Full Adder Using Two X nor Gates Sand Multiplexer Circuit Diagram

III. Results And Discussions

Table1showspowerconsumption, delay and output voltage levels with varying supply voltage [3.3-1.8] V for proposed XNOR gate [Figure 2].Power consumption varies from [500.727-89.931]µ W with variations in supply voltage from [3.3-1.8]Vas shown in Figure 5. Delay varies from[14.466 -23.050]ps with variations in supply voltage from [3.3-1.8]V and has been shown inFigure6.Power consumption has been reduced due to reduced transistor count and reduced capacitance in the XNOR circuit .Short circuit currents are also quite low in the circuit as direct path from supply to ground is eliminated. IthasbeenobservedfromFigure5&6 that power consumption reduces, whereas delay increase with reduction in supply voltage. Table I also show that proposed XNOR gate provide sufficient output voltage levels and noise margin 2V has been obtained with 3.3V supply.

Table 1: Power Consumption, Delay And Output Voltage Levels of Proposed XNOR Gate

Supply voltage (V)	Power consumption (µW)	Output delay (ps)	Minimum level for high output (V)	Maximum level for low output (V)
3.3	500.727	14.466	2.05	0.084
3.0	395.378	15.846	1.84	0.072
2.7	301.417	17.269	1.63	0.0648
2.4	218.996	18.165	1.41	0.05418
2.1	148.329	20.083	1.20	0.04339
2.0	127.452	21.099	1.13	0.04145
1.8	89.931	23.050	0.92	0.03400

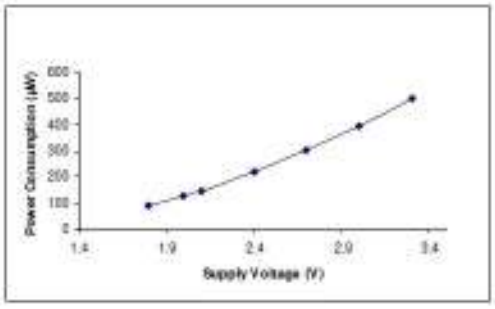

Figure6: Power Consumption Of XNOR Gate With Supply Voltage

Figure3 with variations in supply voltage from [3.3-1.8] V .Power consumption is addition on CMOS inverter and XNOR/XOR cell shows much higher power consumption than single XNOR gate. Minimum level from high output for XOR has also been increased with addition of inverter. Noise margin of circuit is approximately 2V which is near to previous case of XNOR gate.Figure7 show variations of power consumption for XNOR/XOR cell with supply voltage. Figure8 shows input and output waveform results for XNOR/ XOR cell.

Proposed adder circuit shows power consumption of 581.542µW with acceptable level of output. Figure 9shows the input and output wave for full adder circuit. Proposed full adder has less internal capacitance due to reduce number of transistors and shows reduced power consumption. A wide rang e of simulation has been doneform 3.3V to 1.8V to see levels of output signal circuit which shows accept able voltage levels are obtained with proposed circuits.

Table2 Performance Of Proposed Full Adder

Power Consumption (µW)	581.542
Sum delay (ps)	15.1311
Carry delay (ps)	3.372
Minimum level for high sum output (V)	1.97
Maximum level for low sum output (V)	0.24
Minimum level for high carry output (V)	3.2
Maximum level for low carry output (V)	0.32

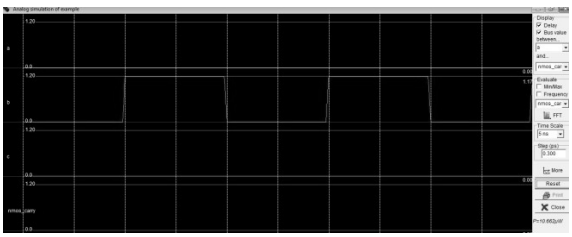

Figure7:Input And Output Patterns For Proposed Full Adder

Table shows comparisons of power consumption, output voltage levels for XNOR gate work and earlier reported circuits.Graph drawn in Figure10 shows that proposed XNOR cell has lowest power consumption among compared circuits.

Table3: Comparisons Of Power Consumption Of Proposed XNOR Cell

XNOR Configuration	Power consumption(µW)	Minimum level for high output (V)	Maximum level for low output (V)
4T[14]	587.63	1.86	0.0006
4T[17]	818.39	1.76	0.0005
4T[15]	1059.2	1.91	0.39
8T[1]	917.66	1.92	0.0004
3T (present work)	500.72	2.05	0.084

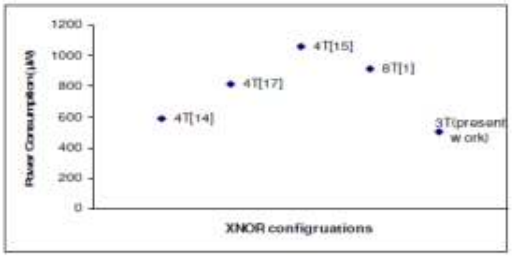

Figure 8: Power Consumptions comparisons For XNOR Gates

Adders reported in[2],[5],[6],[8],[10],[11]have been simulated and comparisons have been presented in Table 5.Graphs drawn in Figure11 shows comparisons of power consumption of proposed circuit and earlier reported circuits. It has been shown that proposed adder show less power consumption than previously reported adders excepted transistors SERF adder [8].Proposed circuits also show superiority in terms of transistor count with earlier reported circuits.

Table4: Power Consumption Comparisons Of Proposed Full Adder

Adder configuration	Power consumption(µW)	Number of transistors for design
TGA20T[6]	1255.54	20
16T adder[2]	591.07	16
10T SERF[8]	531.29	10
22T hybrid adder[10]	1836.4	22

22T HPSC [11]	1533.9	22
18T [5]	617.23	18
8T [present work]	581.542	08

IV. Conclusion

In current work , a new low power XNOR gate with three transistors have been reported which shows power dissipation of 500.7272μW.Comparedwith earlier reported XNOR gates, proposed circuit shows less power consumption and better output signal levels with reduce transistor count . A single bit full adderwith8transistors based on proposed XNOR gate has been presented which show power consumption of 581.542μW with maximum output delay of 15.1311ps. Proposed full adder has been compare with earlier reported circuits and reported circuit shows reduced power consumption number of transistors.

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