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LOW POWER CMOS CIRCUITS USING SLEEP TRANSISTOR TECHNOLOGY

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Abstract-Any computational circuit is incomplete without the use of an Adder. Addition is one of the primary operation in arithmetic circuits. These adder cells commonly aimed to reduce power consumption and delay. The designer's concern for the level of leakage current is mainly aimed at minimizing power dissipation. For portable electronic devices this equates to maximizing battery life. Even though de-activated, these circuits have some leakage current flowing through them. Even if the leakage current is much smaller than the normal operating current of the circuit, it depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate. This device is turned OFF in the sleep mode to cut-of the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance and further reduction of peak of ground bounce noise is possible with used novel technique. The conventional CMOS 28 transistor adder, is considered as Base case. All comparisons are done with Base case. Transistor sizes are specified as a ratio of Width/Length (W/L). It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter. Further, power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. The smallest transistor considered for 130nm technology has a width of 120nm and a length of 100nm. The W/L ratio of NMOS is fixed at 1.2 and W/L of PMOS is 3.8 which is 3.1 times that of NMOS in Design1. The sizing of each block is based on the assumption. These sizing will reduce the standby leakage current greatly because sub-threshold current is directly proportional to the Width/Length ratio of transistor. On the other hand, these reduced sizes reduce the area occupied by the circuit. This will reduce the silicon chip area and in turn reduction in the cost. Size of the sleep transistor is determined by transistor resizing approach. 4 bit adder is implemented using 1 bit adder as reference. The simulation shows that, the 1 bit and 4 bit adders are efficient in terms of standby leakage power, active power and ground bounce noise. Simulations have been performed by using 130 nm CMOS. Electric Tool is used to design the schematic and layout level diagrams. The LT-SPICE Tool will be used for simulation of the Spice code which tests the functionality of generated layout and schematic blocks.

Keywords- Low leakage power, Adder cell, Sleep transistor, Ground Bounce.

I.Introduction

A. Basic Adder Unit

The most basic arithmetic operation is the addition of two binary digits, i.e. Bits. A combinational circuit that adds two bits, according the scheme outlined below, is called a half adder.

A full adder is one that adds three bits, the third produced from a previous addition operation. One way of implementing a full adder is to utilizes two half adders in its implementation.

B. Half Adder:

A half adder is used to add two binary digits together, A and B. It produces S, the sum of A and B, and the corresponding carry out Co. Although by itself, a half adder is not extremely useful, it can be used as a building block for larger adding circuits (FA). One possible implementation is using two AND gates, two inverters, and an OR gate instead of a XOR gate.

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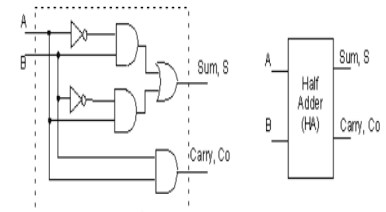


A	B	S	C_o
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 1 (a) Circuit (b) Block diagram;TABLE :Truth Table

C. Full Adder:

A full adder is a combinational circuit that performs the arithmetic sum of three bits: A, B and a carry in, C, from a previous addition. Also, as in the case of the half adder, the full adder produces the corresponding sum, S, and a carry out Co. As mentioned previously a full adder maybe designed by two half adders in series.

The full adder operation can be stated as follows: Given the three 1-bit inputs A, B, and Cin, it is desired to calculate the two 1-bit outputs Sum and Carry, whereSum = (A xor B) xorCin,Carry = A and B + Cin (A xor B)

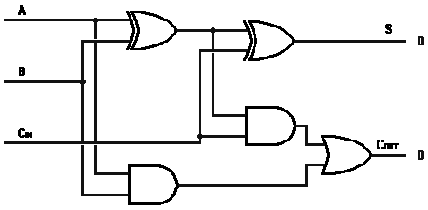


Figure 2: Circuit Diagram of Full Adder

Table 1:Truth Table

A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

D. Conventional Full Adder:

Probably the simplest approach to designing an adder is to implement gates to yield the required majority logic functions. From the table these are:

SUM = A.B.Cin + A.B.Cin + A.B.Cin + A.B.Cin

May be factored as follows:

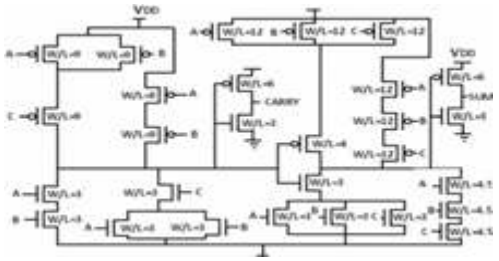
SUM=Cin(AB+AB)+Cin(AB+AB)=A(XOR)B(XOR)Cin

CARRY = A.B + A. Cin + B. Cin= A.B + Cin (A+B)

A full adder can be broken down into three modules by extracting the logical expression for the outputs SUM and Cout using the binary inputs A, B and Cin. Module I essentially perform the XOR (H) and XNOR functions in terms of the inputs A and B.An adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations.The circuit produces a two-bit output, output carry and sum typically represented by the signals Cout and S.

E. Conventional Cmos Full Adder:

In this project I am comparing the three designs of a full adder module.In 1st stage I worked with the conventional full adder module which is a general form of adder this design will not have any particularities about the sizing of the transistor.



F. Design 1 Cmos Full Adder And Design 2 Cmos Full Adder :

Modified adder circuit of Design 2 shown in Figure, the W /L ratio of PMOS is 1.5 times that of W /L ratio of NMOS and each block has been treated as an equivalent inverter. The goal of this design is to reduce the standby

leakage power. Further compared to the Base case, Design 1 an Design 2, ground bounce noise produced when a circuit is connected to sleep transistor is reduced.

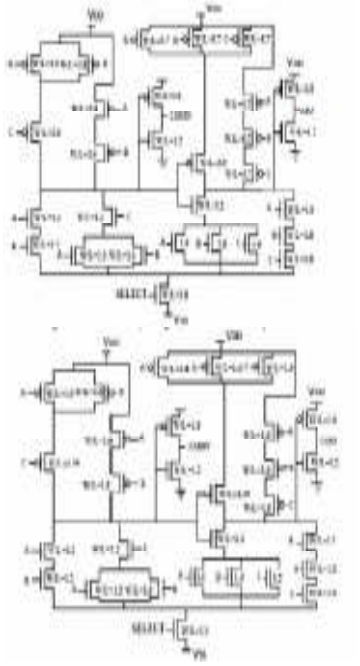


Figure 3: Design 1, 2 CMOS Full Adder

II. Implementation Of Full Adder With Sizing Of A Transistor

we are comparing the three designs of a full adder module. In 1st stage we worked with the conventional full adder module which is a general form of adder this design will not have any particularities about the sizing of the transistor. And then the design 1 full adder with different transistor sizes. And finally will prove that the design 2 is the best and low power and less area consumed solution as compared to the conventional as well as design 1 full adder which differs in transistor sizing. And for all the above three designs we implemented the schematics and layouts with the specified transistor sizing. And implemented the ground bounce noise for the full adder design and calculated the power for that design by lt spice simulation.

A. FullAdder Design: The full adder will be designed with the 28 number of transistors. so that here we are giving a,b,cin as inputs and we will get the sum and carry as the outputs. For that to get the sum and carry as outputs, we need logical xor and logical and and logical or operations. In the above design at left side we have the carry output by doing the andand or operations. and at left side by the xor operations we will get the sum as output. and here we know that if two nmos transistors are in series or if two pmos transistors are in parallel then that is logical AND operation. and if two nmos transistors are in parallel or If two pmos transistors are in parallel then that is logical OR operation.

B. Sizing Effects: In every electronic circuit sizing of a transistor will place a main role.we know that the channel length means the distance between source to the drain. in W/L ratio the W represents the width of the channel and the L represents the length of the channel. If we changed the transistor sizing then the W/L ratio will gets changed and so that I few increased the ratio then the size of the transistor ill increased and the area occupation will gets effects and also it consumes more area as well as power. And hence the design 2 is proved to be better than conventional as well as design 1 full adder. Using the most efficient design that is Design 2 a 4- bit ripple carry adder is designed.

C. Bit Ripple Carry Adder: Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs.Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurance of the corresponding output. Consider a NOT gate, When the input is "0″ the output will be "1″ and vice versa. The time taken for the NOT gate's output to become "0″ after the application of logic "1″ to the NOT gate's input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurance of the carry out (Cout) signal. Circuit diagram of a 4-bit ripple carry adder is shown below.

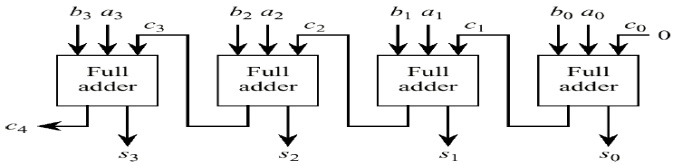


Figure4 : 4-Bit Ripple Carry Adder

Sum out S0 and carry out Cout of the Full Adder 1 is valid only after the propagation delay of Full Adder 1. In the

same way, Sum out S3 of the Full Adder 4 is valid only after the joint propagation delays of Full Adder 1 to Full Adder 4. In simple words, the final result of the ripple carry adder is valid only after the joint propogation delays of all full adder circuits inside it.

D. Sleep Transistor: Leakage power has been increasing exponentially with the technology scaling. In 90nm node, leakage power can be as much as 35% of chip power. Consequently, leakage power reduction becomes critical in low-power applications such as cell phone and handheld terminals. Power-gating is the most effective standby-leakage reduction method recently developed. In the power gating, sleep transistors are used as switches to shut off power supplies to parts of a design in standby mode. Although the concept of the sleep transistor is simple, design of a correct and optimal sleep transistor is challenge because of many effects introduced by the sleep transistor on design performance, area, routability, overall power dissipation, and signal/power integrity. Currently, many of the effects have not been fully aware by designers. This could result in improper sleeper transistor design that would either fail to meet power reduction target when silicon is back or cause chip malfunction due to serious power integrity problems introduced. We have carried out comprehensive investigations on various effects of sleep transistor design and implementations on chip performance, power, area and reliability. In this paper, we shall describe a number of critical considerations in the sleep transistor design and implementation including header or footer switch selection, sleep transistor distribution choices and sleep transistor gate length, width and body bias optimization for area, leakage and efficiency.

A sleep transistor is referred to either a PMOS or NMOS high Vth transistor that connects permanent power supply to circuit power supply which is commonly called “virtual power supply”. The sleep transistor is controlled by a power management unit to switch on and off power supply to the circuit. The PMOS sleep transistor is used to switch VDD supply and hence is named “header switch”. The NMOS sleep transistor controls VSS supply and hence is called “footer switch”. In sub-90nm designs, either header or footer switch is only used due to the constraint of sub-1V power supply voltage.

Although the concept of sleep transistor is simple, optimum sleep transistor design and implementation require optimizing all together the gate length, width and body bias with overall considerations of efficiency, leakage, drive, area and IR-drop effects which are often conflicting and need to be weighted based on application requirements. Increasing Lgate results in higher Vth and hence lower leakage and higher Ion/Ioff efficiency, at price of significant increase of Ron and decrease of Ion. Applying optimal reversed body bias is more efficient and effective alternative to produce a higher efficiency and Ion and lower Ron and Ioff sleep transistor than by increasing Lgate.

a)Sleep Transistor Efficiency (Ion/Ioff): The sleep transistor efficiency is defined by a ratio of drain current in ON and OFF states, i.e. Ion/Ioff. It is desirable to maximize the efficiency to achieve high drive in normal operation and low leakage in sleep mode. The sleep transistor efficiency can be analyzed by SPICE simulations where two high Vth transistors are configured for ON and OFF state respectively to measure Ion and Ioff. A high temperature is set on ON sleep transistor to model high chip temperature in operating mode and a low temperature is set on OFF sleep transistor to reflect the cool situation when the design is in sleep mode. The sleep transistor efficiency varies with gate length, width and body bias.

b)Sleeptransistor Design Considerations:

The sleep transistor implementation introduces extra cost in chip area, routing resource, IR-drop and design complexity. There are also extra power dissipations from sleep transistors, power-gating control logic and power-on/off introduced operations. It is essential to ensure that the leakage reduction from the power gating implementation overwhelms those introduced costs to be worth the effort. To that end, various design considerations and tradeoffs need to be analyzed and handled correctly in the sleep transistor design and implementations. A good sleep transistor design is achieved by optimizing gate length and width, finger size and body-bias based on overall considerations of power efficiency, leakage current, IR-drop, area efficiency and layout impact.

c)Leakage:In electronics, **leakage** may refer to a gradual loss of energy from a charged capacitor. It is primarily caused by electronic devices attached to the capacitors, such as transistors or diodes, which conduct a small amount of current even when they are turned off. Even though this off current is an order of magnitude less than the current through the device when it is on, the current still slowly discharges the capacitor. Another contributor

to leakage from a capacitor is from the undesired imperfection of some dielectric materials used in capacitors, also known as *dielectric leakage*. It is a result of the dielectric material not being a perfect insulator and having some non-zero conductivity, allowing a *leakage current* to flow, slowly discharging the capacitor.Another type of leakage occurs when current leaks out of the intended circuit, instead flowing through some alternate path. This sort of leakage is undesirable because the current flowing through the alternate path can cause damage, fires, RF noise, or electrocution. Leakage of this type can be measured by observing that the current flow at some point in the circuit doesn't match the flow at another. Leakage in a high-voltage system can be fatal to a human in contact with the leak, as when a person accidentally grounds a high-voltage power line.Leakage may also mean an unwanted transfer of energy from one circuit to another. For example, magnetic lines of flux will not be entirely confined within the core of a power transformer; another circuit may couple to the transformer and receive some leaked energy at the frequency of the electric mains, which will cause audible hum in an audio application.

Leakage current is also any current that flows when the ideal current is zero. Such is the case in electronic assemblies when they are in standby, disabled, or "sleep" mode. These devices can draw one or two microamperes while in their quiescent state compared to hundreds or thousands of milliamperes while in full operation. These leakage currents are becoming a significant factor to portable device manufacturers because of their undesirable effect on battery run time for the consumer.

E. Ground Bounce Noise:

Ground bounce is a phenomenon associated with transistorswitching where the gate voltage can appear to be less than the local ground potential, causing the unstable operation of a logic gate.Ground bounce is usually seen on high density VLSI where insufficient precautions have been taken to supply a logic gate with a sufficiently low resistance connection (or sufficiently high capacitance) to ground. In this phenomenon, when the gate is turned on, enough current flows through the emitter-collector circuit that the silicon in the immediate vicinity of the emitter is pulled high, sometimes by several volts, thus raising the local ground, as perceived by the transistor, to a value significantly above true ground. Relative to this local ground, the BASE voltage can go negative, thus shutting off the transistor. As the excess local charge dissipates, the transistor turns back on, possibly causing a repeat of the phenomenon, sometimes up to a half-dozen bounces.Ground bounce is one of the leading causes of "hung" or metastable gates in modern digital circuit design. This happens because the ground bounce puts the input of a flip flop effectively at voltage level that is neither a one or a zero at clock time, or causes untoward effects in the clock itself.

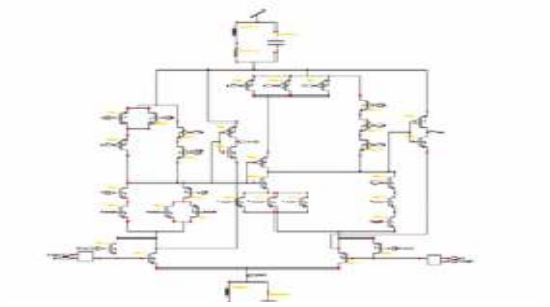


Figure 5: Fulladderwith Ground bounce technology

III. Results

A. Conventional 1-bit full adder Schematic & Layout:

The schematic, layout of 3 inputs (a, b, c) and 2 outputs (sum &Cout) conventional CMOS 1-bit Full Adder is as shown in Fig. This is designed in Electric tool.

Figure 6:Schematic, Layout of Conventional 1-Bit FullAdder

The conventional CMOS 1-bit Full Adder schematic and layoutsimulation results which are observed in LT-SPICE tool are as shown in Fig.

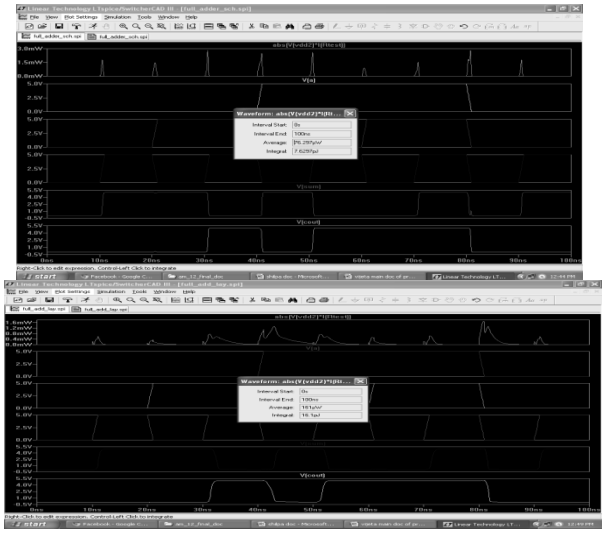


Figure 7:Schematic, Layout Simulation Results

B. Design 1 CMOS 1-bit full adder Schematic & Layout using Sleep Transistor:

In design 1 a sleep transistor is added between the actual ground and the virtual ground to reduce the power dissipation and also resizing of transistors. The Design 1 CMOS 1-bit Full Adder schematic, layout with 3 inputs and 2 outputs after re-sizing is as shown in Fig. This is designed in Electric tool.

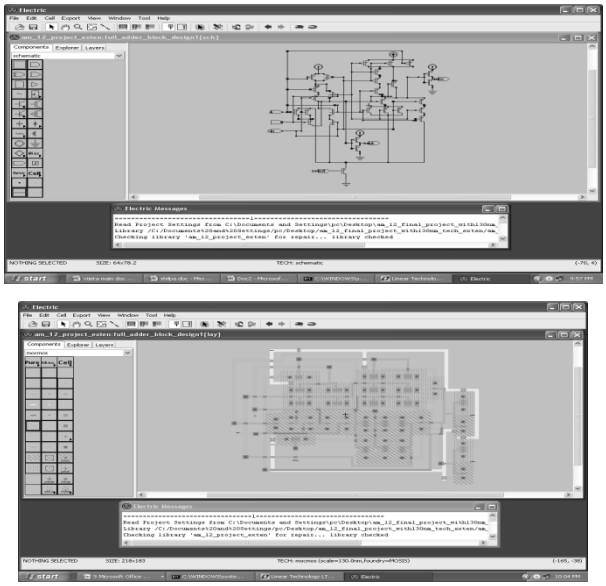


Figure 8: Schematic and layout of Design 1 CMOS 1-Bit Full Adder using Sleep transistor

The Design1 1-bit Full Adder schematic, Layoutsimulation results which are observed in LT-SPICE tool are as shown in Fig

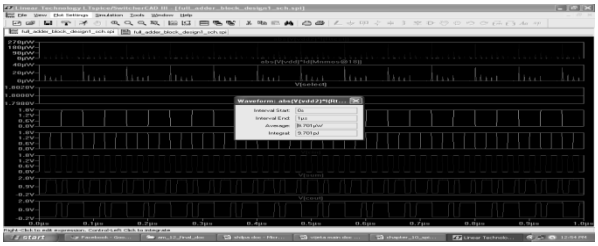


Figure 9: Schematic Simulation Results of Design 1 CMOS 1-Bit Full Adder using Sleep transistor

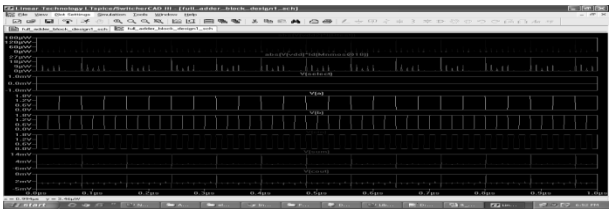


Figure 10: layout Simulation Results of Design 1 CMOS 1-Bit Full Adder using Sleep transistor; The above figure shows the output is when select is logic high i.e., vselect=1

Figure 11: layout Simulation Results of Design 1 CMOS 1-Bit Full Adder using Sleep transistor; The above figure shows the output is when select is logic low i.e., vselect=0

C. Design 2 1-bit full adder Schematic & Layout:

In design 2 the full adder is further modified by resizing of transistor to still reduce the power dissipation. The Design 2 CMOS 1-bit Full Adder schematic, Layout with 3 inputs (a, b, c) and 2 outputs (sum &Cout) after further re-sizing is as shown in Fig. This is designed in Electric tool.

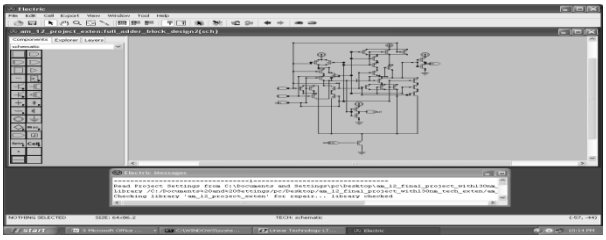


Figure 12:Schematic, Layout of Design 2 CMOS 1-Bit Full Adder using Sleep transistor

The Design2 1-bit Full Adder schematic,Layoutsimulation results which are observed in LT-SPICE tool are as shown in Fig

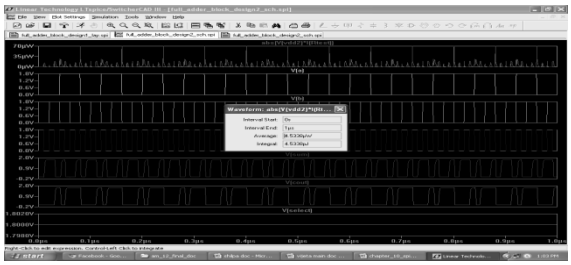


Figure 13: Schematic Simulation Results of Design2 CMOS1-Bit FullAdder using Sleep transistor.

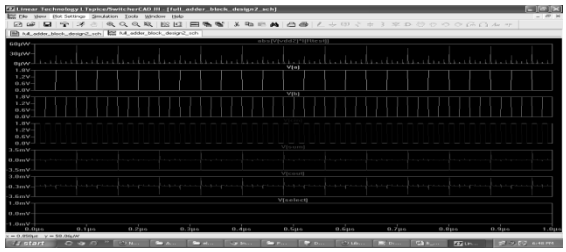


Figure 14: Layout Simulation Results of Design2 CMOS1-Bit FullAdder using Sleep transistor; The above figure shows the output is when select is logic high i.e., vselect=1

Figure 15: Layout Simulation Results of Design2 CMOS1-Bit FullAdder using Sleep transistor; The abovefigure shows the schematic results when select is logic low i.e., vselect = 0

From the above schematics and layouts results the Design 2 is most efficient. So, using design 2 i.e., the proposed solution 4-bit ripple carry adder is designed

D. 4-Bit Ripple Carry Adder:

Therefore it is proved that Design 2 is most efficient. So, using Design 2 4-bit ripple carry adder is designed & following shows the schematic & layout of 4-bit ripple carry adder. The schematic of 4-bit ripple carry adder is shown in below figure

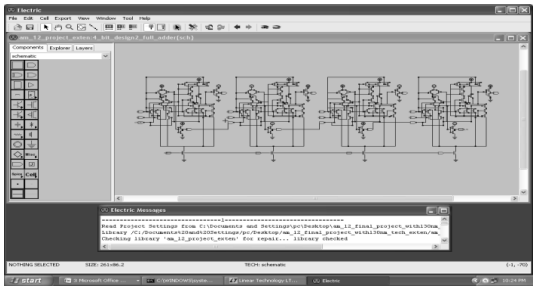


Figure16 : Schematic of 4-bit ripple carry adder using Sleep transistor

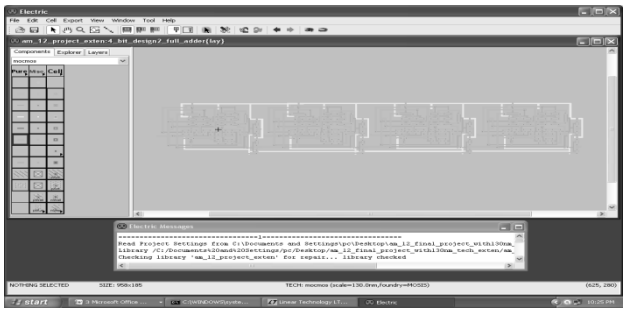


Figure 17: Layout of 4-bit ripple carry adder using Sleep transistor

The schematicsimulation result of 4-bit ripple carry adder which are observed in LT-SPICE tool are as shown in Fig

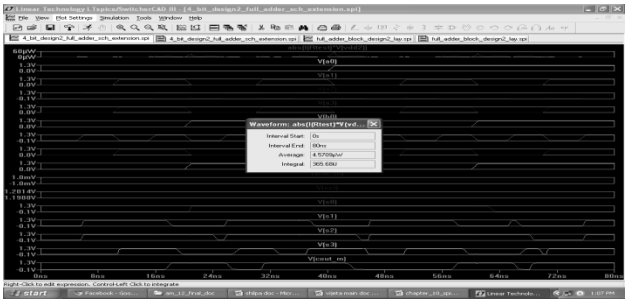


Figure 18: Schematic Simulation Results of 4-Bit Ripple Carry Adder using Sleep transistor

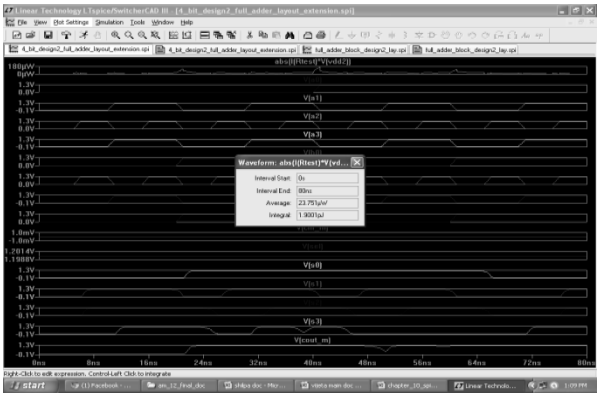


Figure 19:Layout Simulation Results of 4-Bit Ripple Carry Adder using Sleep transistor

E. Ground Bounce Noise Schematic & its Result:

One bit full adder is divided into two separate but cascaded blocks. The first is the carry generation block and the following is the sum generation block. Separate sleep transistors are added at the bottom of the blocks. The below figure shows the schematic of ground bounce noise reduction using the efficient design. This is designed in Electric Tool.

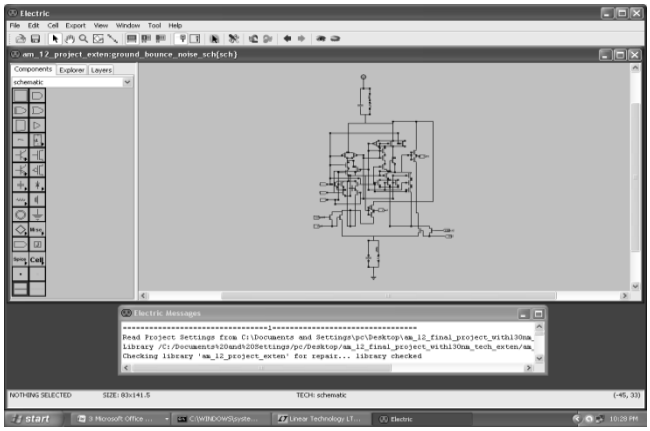


Figure 20: Schematic results of Ground Bounce Noise Reduction

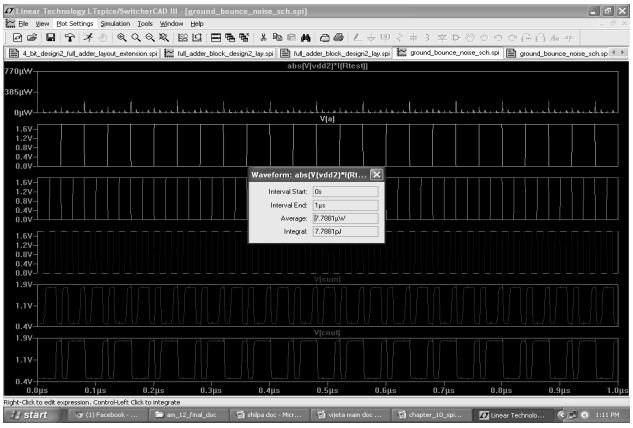


Figure 21: Simulationresults of Ground Bounce Noise Reduction

IV. Conclusion

Table 2:Comparision of Power Dissipation

DESIGN TYPE	SCHEMATIC (Power Dissipation)	LAYOUT (Power Dissipation)
Conventional full adder	76.297µW	161µW
Design 1	9.701µW	24.165µW
Design 2	4.5338µW	18.11µW
4- Bit Ripple Carry Adder	4.5709 µW	23.751µW

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