Indian J.Sci.Res. 14 (2): 262-269, 2017 ISSN: 2250-0138 (Online)

# COMPARATIVE ANALYSIS OF Si AND 4H-SiC D-MOSFETs

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## ABSTRACT

**In the generation, storage and distribution cycle of the electric energy, the workhorse is the power transistor (MOSFET). These power transistors are developed on silicon semiconductor technology. To overcome the limitation of silicon technology, such as low band gap, less blocking voltage capability, low switching frequency, 4H-SiC D-MOSFETs are the material of choice. The 4H-SiC D-MOSFETs with wide band gap semiconductors can be able to operate at higher blocking voltage, high switching frequency, low-specific ON resistance and also it will allow to operate at very high temperatures. This paper aims on various design structures of 4H-SiC D-MOSFETs and its behavioral study for circuit application. The extracted parameters of D-MOSFETS are ON-resistance, blocking voltage, the sensitivity of temperature by using the TCAD simulations are presented to prove their characteristics.**

**KEYWORDS:** 4H-SiC DMOSFET, Blocking Voltage, Switching Frequency.

Power transistors like bipolar junction transistors (BJTs), insulated-gate bipolar transistors (IGBTs) and power metal-oxide-semiconductor field-effect transistors (MOSFETs) are based on silicon semiconductor technology having wide usage in the field of power electronics and power systems. Power MOSFETs are capable of handling higher voltage and current levels. The great usage within the power-supply community is of power MOSFETs, because of their ease of drive along with their low switching losses makes them the absolute choice for high switching frequency applications. These power MOSFETS are being used in resonant converter and inverters with the maximum switching frequency upto 1 MHZ respectively. Recently, there is an increase in demand for power devices can withstand a very high voltage and higher switching frequency. These devices are mostly used for advanced power conversion systems (DC-DC, DC-AC). Power MOSFETs can be operating at a high temperature over $150^0$C. Silicon based devices are unable to operate properly at high temperature and high switching frequency, while the Silicon based MOSFET operating at high degree temperature requires costly cooling systems and display units. This may increase the overall cost, size and weight of the power conversion system. The main feature of Silicon carbide and gallium nitride semiconductor materials is wide band gap, which has the following advantages for power electronic designers are:

- a lower intrinsic carrier concentration (10-35 orders of magnitude),
- a higher electric breakdown field (4-20 times),
- a higher thermal conductivity (3-13 times),
- and a largely saturated drift velocity (2-2.5 times), when compared to silicon.

**Table I: Material Parameters of Silicon and Silicon Carbide**

| Material | Material Properties | | |
|---|---|---|---|
| | Energy Band gap | Critical/Avalanche Breakdown Field | Thermal Conductivity |
| Silicon | 1.10 | 0.3 | 1.5 |
| 3C-SiC | 2.20 | 1.2 | 4.5 |
| 4H-SiC | 3.26 | 2.0 | 4.5 |
| 6H-SiC | 3.00 | 2.4 | 4.5 |

From Table I, Silicon Carbide band gap energy of 2.2-3.3eV is larger than that of Si. 150 poly types SiC devices are introduced by many researchers, but only the 6H- and 4H-SiC poly types are available commercially. The 4H-SiC are primarily preferred for power devices because of its high carrier mobility and low dopant ionization energy. Also the high electric break-down field of SiC allows for thinner epitaxial layer to support the high blocking voltage in power devices. A 5000-V power device would require only 40-50µm drift layer, as opposed to almost 500µm in the case of silicon. This smaller drift layer leads to low drift resistance, hence low forward drop, conduction losses and thermal conductivity is 5W/cmK,allows for high junction temperature operation and efficient thermal management [ Okayama et. al., 2008] [ Chen et. al., 2016].

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## DEVICE STRUCTURES AND CHARACTERISTICS

Fig.1 Shows a simplified cross-section of the 4H-SiC DMOSFET. Here the channel length is 0.5µm, and the drift layer thickness is 10µm. When a positive gate bias, more than the threshold voltage is applied, the MOS channel turns on and electrons flow laterally from the n+ source, through the MOS channel on the implanted p-well. Then Electron flow through the JFET region formed by two adjacent p-well regions and, finally, through the lightly doped n⁻ drift region into the backside drain. The MOS channel length is defined by the p-well and n+ source region; the MOS channel disappears when the gate electrode is shorted to the source or when a negative gate bias is applied. The total on-resistance of the 4H-SiC DMOSFET consists of channel resistance($R_{ch}$), JFET resistance($R_{JFET}$), spreading resistance($R_{spd}$), drift-layer resistance ($R_d$) and substrate resistance($R_{sub}$) When the MOS channel off, the 4H-SiC DMOSFET behaves as a 4H-SiC PiN diode. The device supports the high voltage by reverse biased pn junction formed by the implanted p-wells and the thick n⁻ drift layer.

**Structure 1: Characteristics**

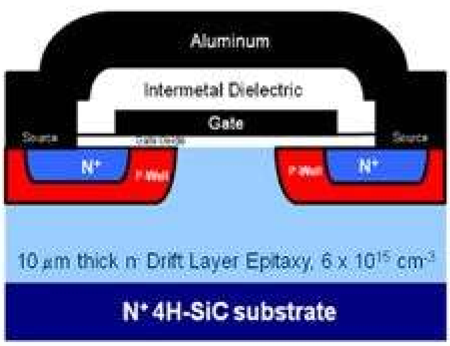
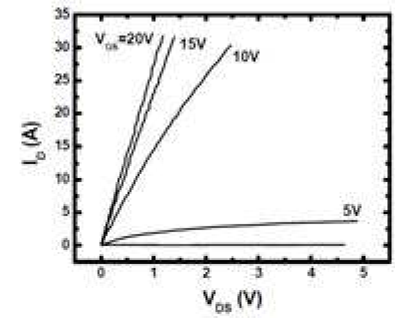



**Figure 1: A simplified cross-section of the 4H-SiC DMOSFET.**

The on-state I-V characteristics of the SiC DMOSFET designed by Sei-Hyung Ryu et al illustrated in Fig.1, has measured at room temperature. When $V_{GS}$ was 20V the specific on-resistance was 3.7mΩ-$cm^2$, as the $V_{GS}$ was reduced to 15V specific on-resistance was increased to 4.3mΩ-$cm^2$. The forward voltage drop at an $I_D$ of 30A was 1.1V with a $V_{GS}$ of 20V and 1.3V with a $V_{GS}$ of 15V (Fig. 2a) The blocking voltage was 1500V (Fig. 2b).

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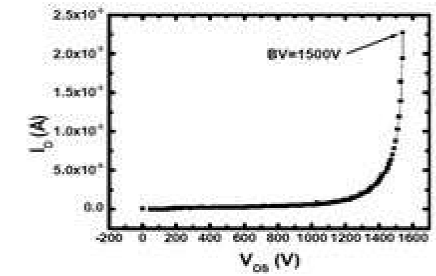


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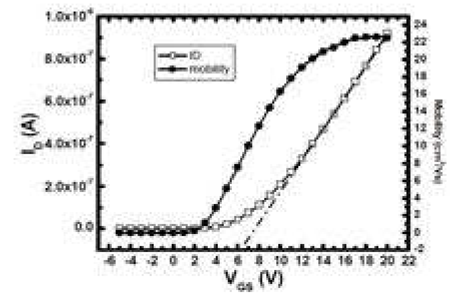



**(c)**

**Figure 2: (a) On-state I-V Characteristics (b) Blocking characteristics(c) $I_D - V_{GS}$ characteristics of the DMOSFET.**

**Structure 2: Characteristics**

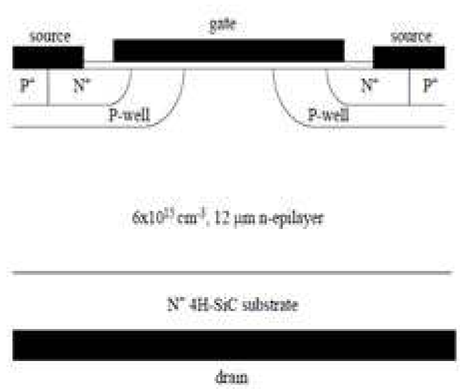
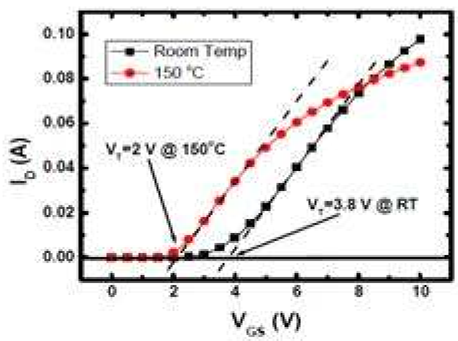



**Figure 3: Simplified cross-section of the 4H-SiC DMOSFET.**

The structure designed by Sei-Hyung Ryu et al shown in Fig.3, the $I_D$ –$V_{GS}$ and blocking characteristics of the power MOS with an active area of $0.0278cm^2$ is shown in Fig.4(a). Here the ($V_{DS}$) was set at 50 mV, the extracted $V_{th}$ at room temperature was 3.8V. The device is normally off and showed a stable avalanche characteristic at a ($V_{DS}$) of 2kV (Fig. 4(b)) with a $V_{GS}$ of 0V.

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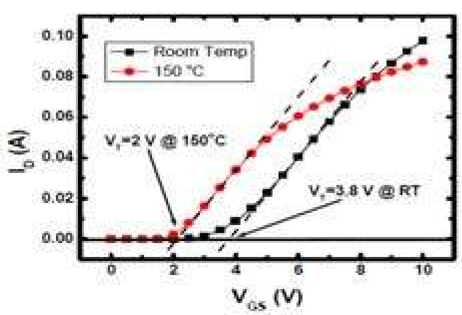



**(b)**

**Figure 4: (a) $I_D - V_{GS}$ characteristics of the DMOSFET (b) Blocking characteristics of the DMOSFET.**

**Structure 3: Characteristics**

The designed structure of Sumi Krishna swami et al depicted in Fig.5, the $I_D$ versus $V_{GS}$ characteristics having (W/L = 150µm/150µm), was measured, here the drift layer thickness was 85µm and the measured threshold voltage was 4V and the blocking voltage of the device was 10-kV which are depicted in the (Fig. 6).

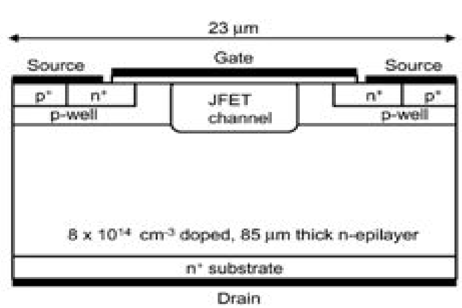
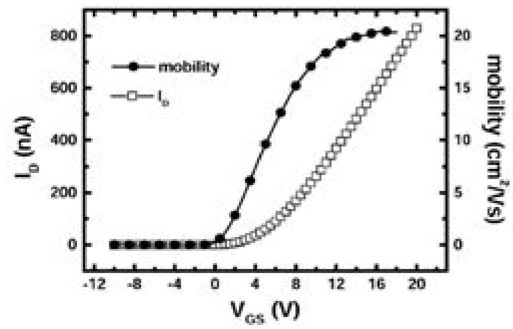



**Figure 5: Cross-section of the Power MOSFET.**

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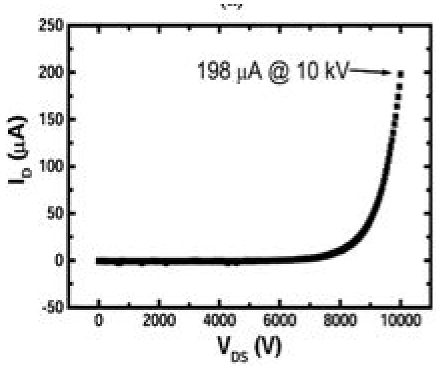



**(b)**

**Figure 6: (a) $I_D$ *versus* $V_{GS}$ curve of the Power MOSFET (b) A leakage current of 198 µA at a drain bias of 10 kV.**

**Structure 4: Characteristics**

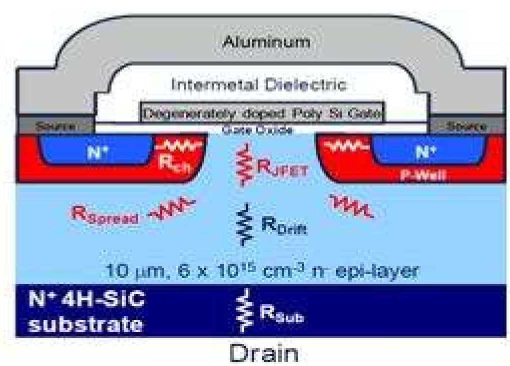
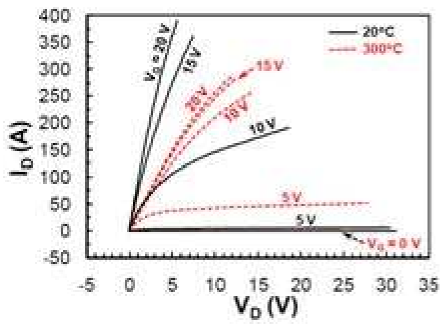



**Figure 7: cross-section of the Power DMOSFET**

Fig.7 shows the 4H-SiC MOSFET structure designed by Lin Cheng et al.in the chip size was of 7mm×8mm while active conducting area was of 0.4 . Below figure resembles the on-state I-V characteristic of the MOSFET which were measured from the range of $20^0$ to $300^0$ in pulsed mode using a Tektronix 371 curve tracer. The graph also depicts the temperature dependence of forward characteristics at a $V_G$ of 20V. The SiC MOSFET was able to conduct over 200 A at temperature up to $300^0$. Under a gate bias of 20V and $I_D$ of 20A, the

($R_{ON,SP}$) is increased from 3.4 mΩ.cm$^2$ at 20$^0$ to 11.6 mΩ.cm$^2$ at 300$^0$ while it increased from 4.7 mΩ.cm$^2$ at 20$^0$ to 14.2 mΩ.cm$^2$ at 300$^0$ at $I_D$ of 200A (fig. 8).

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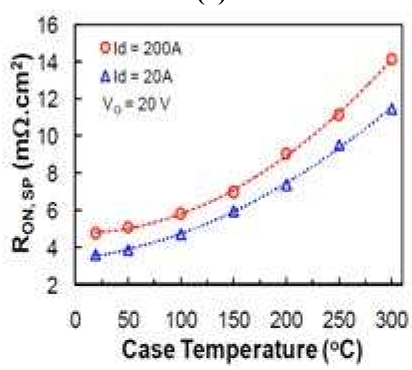



**(b)**

**Figure 8: (a) On-state I-V characteristics of the Power DMOSFET, at 20$^0$ and 300. (b) Specific on-resistance as a function of temperature.**

**Structure 5: Characteristics**

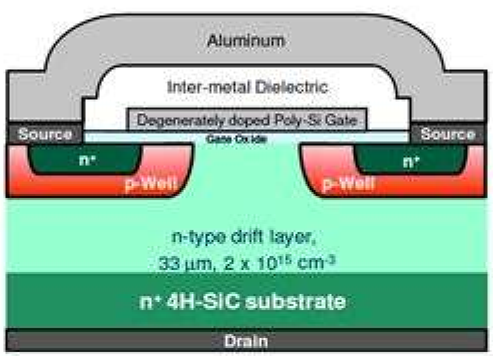
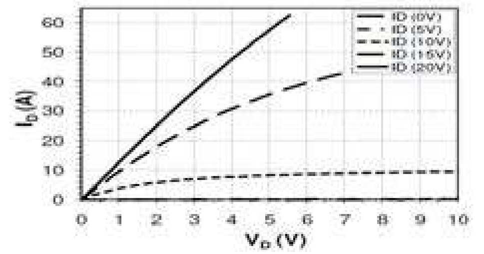



**Figure 9: Simplified cross-section of a 3300V, 30 A 4H-SiC DMOSFET.**

Fig.9 illustrates the structure designed by Lin Cheng et al, described about a Power DMOSFET having device size of 200µm/200µm. The I-V characteristics of the device and the blocking voltage characteristic are depicted in the below figure, the device conducts 39 A at a drain bias $V_{DS}$ of 2.97V with a $V_{GS}$ of 20V and 31.7 A at a $V_{DS}$ of 3.68V with a $V_{GS}$ = 15V . The specific on-resistance ($R_{ON,\ SP}$) was 35.3mΩ.cm$^2$ and 27mΩ.cm$^2$ at $V_{GS}$ values of 15V and 20V, respectively (fig. 10).

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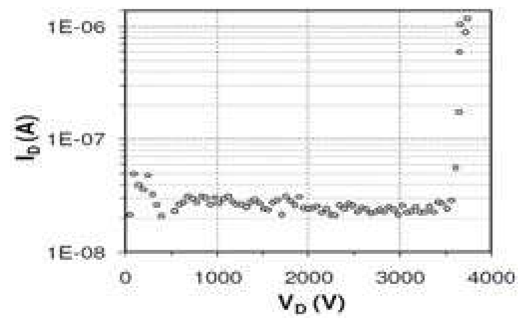



**(b)**

**Figure 10: (a) On-state I-V characteristics of the 3300V, 30A 4H-SiC DMOSFET (b) Off-state I-V characteristics of the 3300V, 30A 4H-SiC DMOSFET.**

**Structure 6: Characteristics**

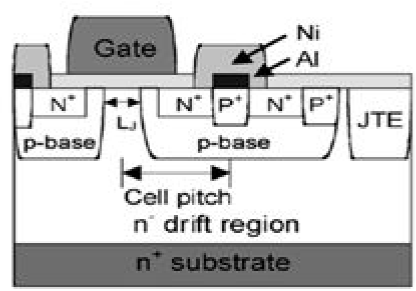
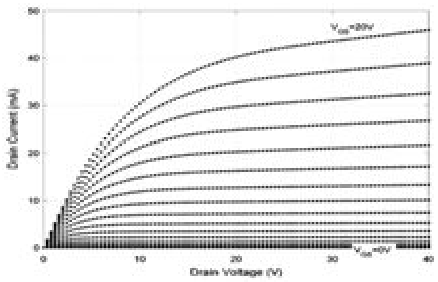



**Figure 11: Schematic cross section of the short-channel DMOS cell**

The structure designed by M. Matin et al shown in Fig.11, a self-aligned process is introduced to produce short-channel length to ≤ 0.5µm, where the specific on-resistance of the MOSFET channel is proportionally reduced, significantly enhancing performance. The JFET region width was 6µm, drift layer thickness was 20-µm, with channel length of 0.5µm (Fig. 12(a,b))

**Structure 7: Characteristics**

Fig.13 shows the structure designed by A. Saha et al. have described a short-channel 4H-SiC power DMOSFET with several structural modifications to reduce the specific ON-resistance. The modification were: (1) a heavily doped n-type current-spreading layer beneath the p-base; (2) a heavily-doped JFET region with narrow JFET width; (3) a "segmented" base contact layout; (4) tighter alignment tolerances to reduce cell pitch. Fig.14(a,b) shows the variation of blocking voltage and specific ON-Resistance characteristics.

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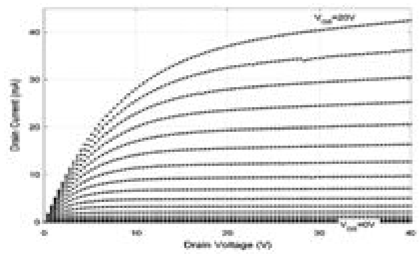



**(b)**

**Figure 12: (a) ON-State characteristics of the DMOSFET with $L_J$ = 8µm. (b) ON-State characteristics of the DMOSFET with $L_J$ = 6µm.**

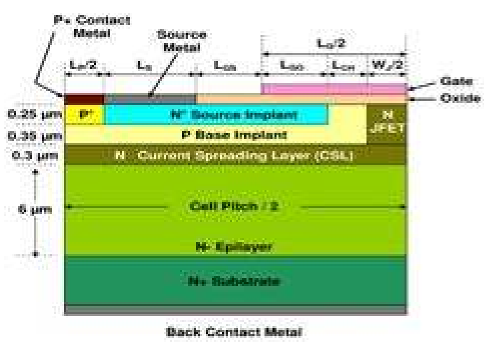
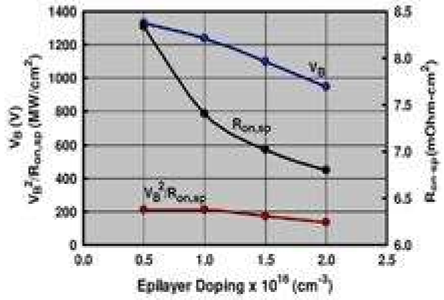



**Figure 13: A cross-sectional view of the DMOSFET cell**

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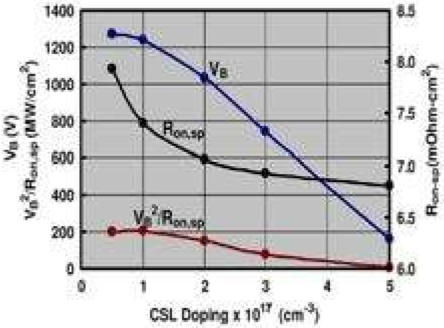
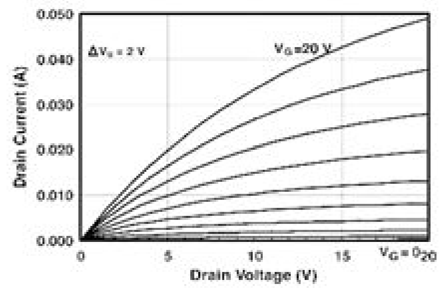



**(b)**

**Figure 14: (a) Variation of Blocking voltage ($V_B$), Specific ON-resistance ($R_{ON,SP}$) with epilayer doping. (b) Variation of $V_B$, $R_{ON,SP}$ with CSL doping.**

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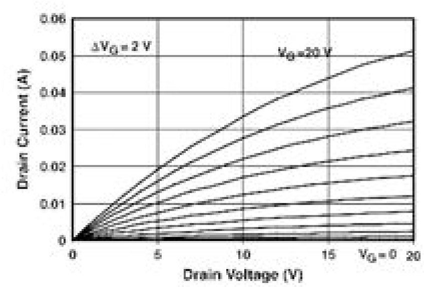



**(b)**

**Figure 15: (a) ON-state characteristics of the device with JFET length of 1µm. (b) ON-state characteristics of the device with JFET length of 1.5 µm.**

**Structure 8: Characteristics**

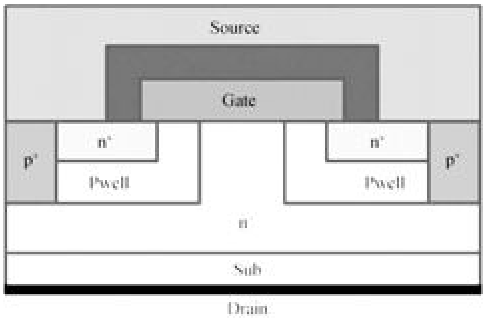
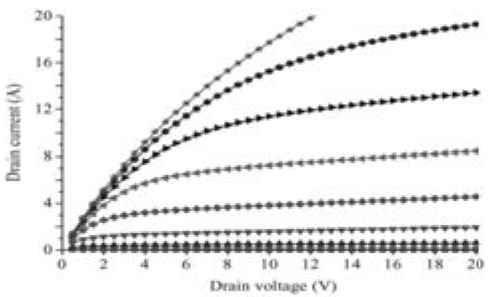



**Figure 16: Device Cross-sectional view of the 3300 V 4H-SiC DMOSFET.**

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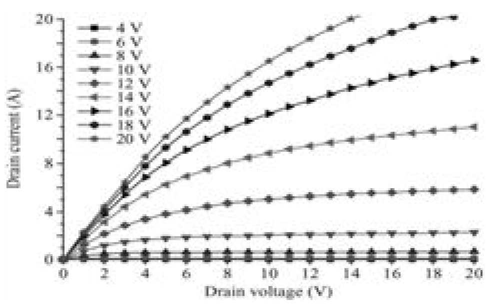



**(b)**

**Figure 17: (a) I-V Characteristics. (b) $I_D - V_D$ characteristics of the 3300 V 4H-SiC MOSFET**

Fig.16 depicts the 4H-SiC DMOSFET designed by Huang Runhua et al.in, had a breakdown voltage higher than 3300 V. The epilayer thickness was 33µm with a doping of $2.5\times10^{15}cm^{-3}$. The drain current $I_D$ = 5A at $V_G$ = 20V corresponding to $V_D$ = 2.5V (Fig. 17(a,b))

**Table II: Comparision of different Structure Parameters**

| Structure | Drift layer Thickness (µm) | $R_{on,sp}$(mΩ-$cm^2$) | Blocking Voltage (kV) |
|---|---|---|---|
| Structure 1 | 10 | 3.7 | 1.5 |
| Structure 2 | 12 | 10.3 | 2 |
| Structure 3 | 85 | 123 | 10 |
| Structure 4 | 10 | 11.6 | 1.2 |
| Structure 5 | 33 | 27 | 3.3 |
| Structure 6 | 20 | 27 | 2 |
| Structure 7 | 7 | 6.95 | 1 |
| Structure 8 | 32 | 27 | 3.3 |

## SIMULATION RESULTS

The 4H-SiC DMOSFET structure design and simulation were carried out by using the T-CAD simulation tool. The designed structure shown in (Fig. 18)

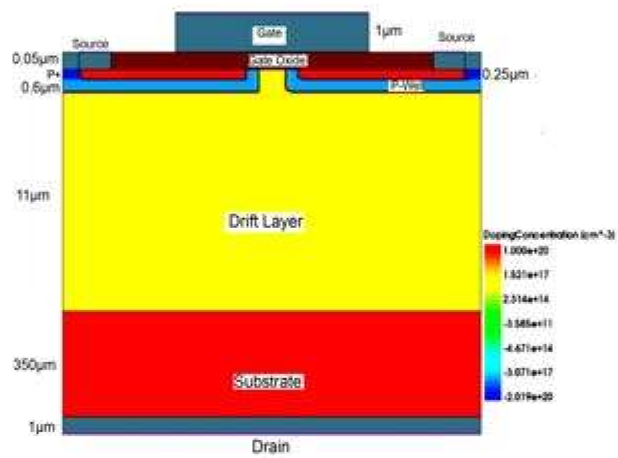
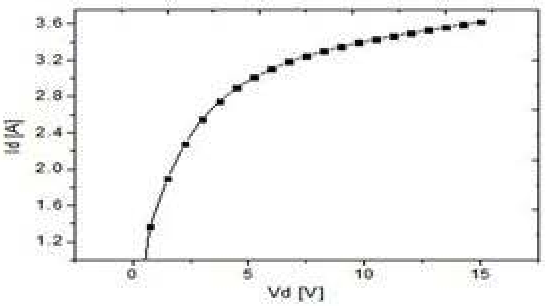



**Figure 18: Designed structure of 4H SiC D-MOSFET**

The results obtained for the channel length 0.5µm and JFET width of 1µm of this structure are illustrated in Fig.19(a) $I_D$-$V_D$ characteristics with 0-15 V drain voltage and 3.6 A maximum drain current. Similarly the simulation results achieved for $I_D$-$V_G$ characteristics shown in Fig.19(b), by changing the gate voltage from 0-20V. By the way of increasing the drift layer the blocking voltage can be increased.

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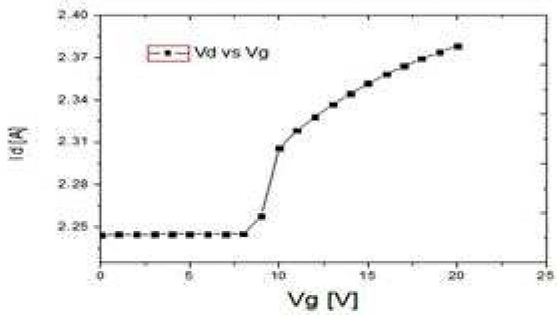


**(b)**

**Figure 19: (a) I-V Characteristic. (b) $I_d$ versus $V_g$ characteristic with channel length of 0.5 µm and JFET region of 1 µm.**

## CONCLUSION

The paper presents the compartive analysis of different D-MOSFETs structures and simulation results of existed D-MOSFET structure. The main applications of these SiC devices can be operate at high-temperature with wide band gap semiconductors in power conversion technology. Future scope of this work focusing on the following variants in the structure; By increasing thickness of drift layer, the SiC device can have more blocking voltage and Specific On-state resistance can be reduced by minimal the width of JFET. These variants may improve overall performance of the device.

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