Indian J.Sci.Res. 17(2): 463 - 466, 2018 ISSN: 0976-2876 (Print)
ISSN: 2250-0138(Online)

DESIGN OF A NOVEL FLASH ANALOG TO DIGITAL CONVERTER FOR LOW POWER AND HIGH SPEED APPLICATIONS

[1]K.Sandeep Kumar,[2]D.Manirathnam Reddy
[1,2]Department of Electronics and Communication Engineering,Aurora's Scientific,Technological And Research Academy,Hyderabad,Telangana,India-500005

Abstract- Analog to Digital Converters(ADCs) are the fundamental building blocks which are used in many digital signal applications such as a data storage, read channel and an optical receiver, because they act as the interface between the real world analog signal and today's digital signal processor applications .In this paper we designed a 3-bit Flash Analog to Digital Converter (ADC) using 180 nm CMOS Technology. For achieving high speed ,a flash type ADC was used . Resolution, speed of response, and power consumption are the three major key parameters for an Analog-to-Digital Converter (ADC). The flash ADC is operated at 3-bit precision with analog input voltage of 0 to 1.8V.The thermometer code-to-binary code encoder has become the bottleneck for ultra-high speed flash ADCs. The speed of respose of the fat tree encoder is improved by almost twofold when using this fat tree encoder which gives an effective solution for modern ultra-high speed ADCs.The ADC has been designed, implemented and analyzed in standard gpdk180nm technology library using Cadence tool.

Keywords- Flash ADC, TC, BC, Fat Tree Encoder,Techlib 180nm Cadence suite.

I. Introduction

A flash ADC is often used for high-speed applications. Many applications require high speed ADCs with a conversion speed of one clock cycle. Flash analog-to-digital converters also known as parallel ADC, holds its importance because of high speed operation. The conversion speed in flash ADC is only one clock cycle and hence is the fastest ADC architecture available and is limited only by comparator and gate propagation delays. Resolution, speed, and power consumption are the three key parameters for an analog-to-digital converter (ADC). Low power ADC architectures are implemented with pipelined, successive approximation, and sigma-delta modulators. These are all useful for the medium speed conversion and high resolution applications. On the other hand, the flash architecture is suitable for high speed conversion and low resolution applications due to its parallel architecture.

A flash analog-to-digital converter (ADC) is known for its high speed operation. An n hit ADC's front-end consists of N - 1 (where N = 2^n) voltage Comparators, comparing fully parallel the incoming analog signal with N – 1 reference voltages. The comparators produce the digital thermometer-code (TC), and the remaining back-end of a flash ADC consists of a thermometer code-to-binary code encoder, as shown in Figure I .In this paper, the authors present the fat tree TC-to-BC encoder that is highly suitable for the ultra-high speed flash ADCs. The main advantage of the fat tree encoder over the other encoders is the high encoding speed. Also the fat tree encoder consumes less power compared with the ROM encoder. However, the fat tree layout design is more difficult and time consuming than the ROM layout design.

II. Flash ADC Architecture

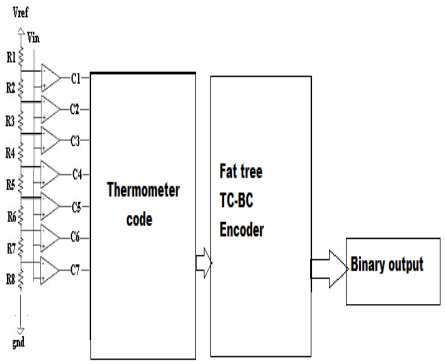

Fig.1. Flash ADC Architecture

The Fig. 1. Shows a typical flash ADC block diagram. For an "3" bit converter, the circuit employs 2^3-1= 7 comparators. A resistive divider with 2^3 = 8 resistors provides the reference voltage The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is "0".

The 2^N-1 comparators produce the thermometer code (TC), it is called thermometer code because as the amplitude of the analog input increases the number of ones in the output increases linearly which is similar to the mercury rise in the thermometer, and the digital encoding network converts 2^N-1 inputs to N bit binary code (BC).

[1]Corresponding Author

A. Fat Tree Encoder

After the comparators produce a thermometer code, it is converted to binary code. The TC-to-BC encoding is carried out in two stages in the fat tree encoder. The first stage converts the thermometer code to one-out-of-N code. The one-out-of-N code is same as an address decoder output. This code conversion is done in N bit parallel using N gates. The second stage converts the one-out-of-N code to binary code using the multiple trees of OR gates.

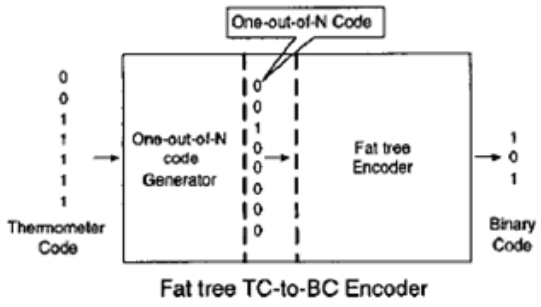

Fig 2:The two stage fat tree TC to BC Encoder

III. DESIGN AND IMPLEMENTATION

A. The Resistor String

The 3 bit flash ADC, needs 2^3 resistances . The two extreme resistors are calculated to delimit the voltage input range. Each resistor divides the reference voltage to feed a comparator. The higher the resistance value is, the weaker the current is consumed in the device. That is why a high resistance will minimize power dissipation. Nevertheless, we have to put a reasonable value for this resistor string it should stand lower than the input resistance of the comparators. We expected to convert any voltage between 0 and 1.8 V. In general, the voltage division takes place as follows:

Va = (M*Vref)/2^n …… (1)

Where,

M = No., of resistors at which voltage division occurs.

n = No., of bits.

2^n= Total No., of resistors used.

The Table 1 show the voltage division for resistor string with reference voltage is taken to be 1.8 V.

Table 1:Voltage division occurs as follows.

M *	Va*= (M*Vref)/2n
	1.575 V
Tap 6	1.35 V
Tap 5	1.125 V
Tap 4	0.9 V
Tap 3	0.675
Tap 2	0.45
Tap 1	0.225

*M= Resistor tap Number & Va=Voltages of each resistor tap.

The design of resister string for proposed Flash ADC is done using schematic approach in cadence as shown in fig.3

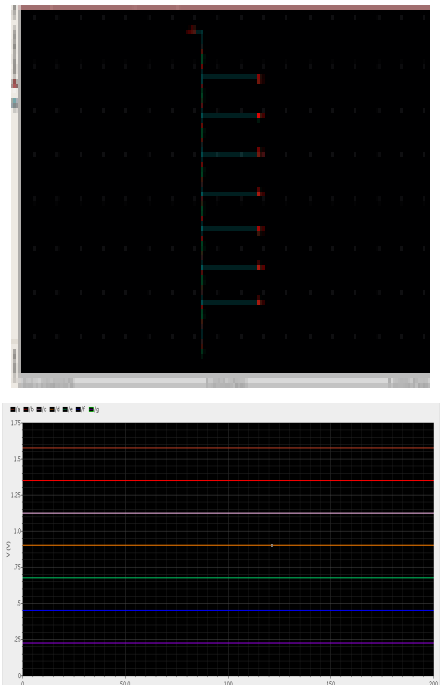

Fig.3 The design of resister string for proposed Flash ADC

B. The Comparator

The proposed flash ADC consists of comparator as one of the important component, this comparator is designed in such a way that which is less immunity for noise and with high common mode rejection ratio. Hence, the Differential Amplifier is used to achieve the same.

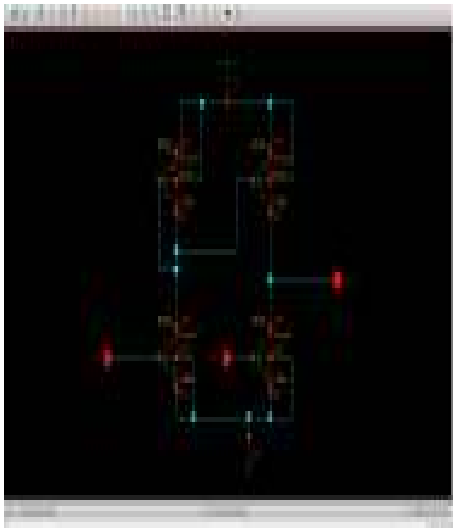

Fig.4 Comparator

2^3-1=7 differential amplifiers are used as comparators in 3-bit flash-ADC architecture. When the input signal voltage is less than the reference voltage, the comparator output is at logic '0'.when the input signal voltage is higher than the reference voltage, the comparator output is at logic '1'. The comparators give the 7 levels of outputs in terms of reference voltage.

IV. Experimental Results

This Section clearly discuss about the simulation results of above said three important components of flash ADC, the work is carried out on cadence virtuoso the simulation is done using spectra.

The schematic simulation of 3 bit Flash ADC using Cadence tool is shown in Fig.

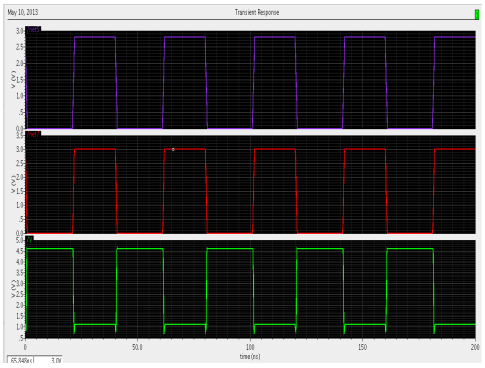

Fig 5 schematic simulation of 3 bit Flash ADC

Fig. shows transient response for Vin = 1.6V and Fat tree encoder output will be "111".

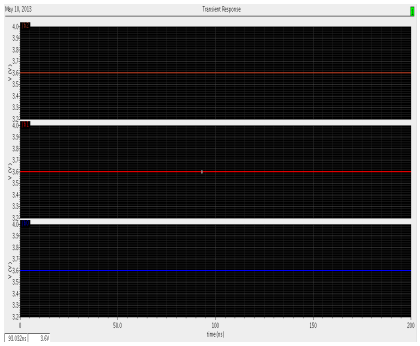

Fig 6 transient response for Vin = 1.6V

Fig. shows transient response for Vin = 1V and

Fat tree encoder output will be "100".

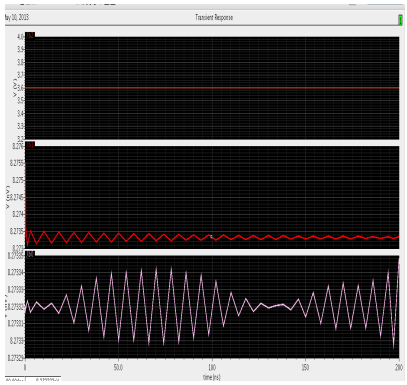

Fig 7 transient response for Vin = 1V

Fig. shows transient response for Vin = 1V and

Fat tree encoder output will be "100".

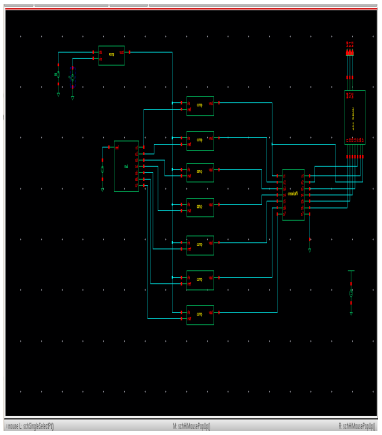

Fig 8 outputs for analog input of 0 to 1.8V and 10 M Hz input frequency using sample and hold Circuit.

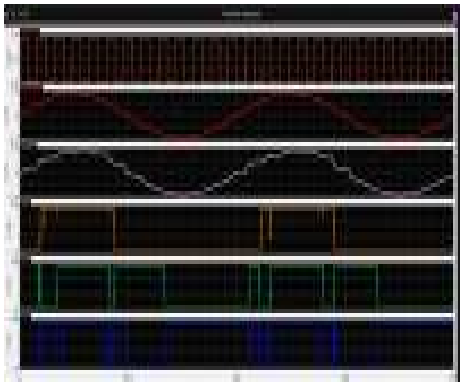

Fig 9 Flash ADC outputs for analog input of 0 to 1.8V and 10 M Hz Input frequency.

Results

Specifications Summary of ADC

specifications	With Fat Tree Encoder	Normal Encoder
Technology	180ηm	180ηm
Analog voltage, Vin	0 to 1.8V	0 to 1.5 V
Reference voltage, Vref	1.8V	1.5 V
Vdd	3.6V	1.3 V
Resolution	3-bits (224.28mV/LSB)	3-bits
Speed	2.41 GS/sec	----
Power Dissipation	24.73 mW	36.237 mW

V. Conclusion

This Paper discusses the overall contribution of the 3-bit ADC. The schematic of register stage, sample and hold circuit, comparator stage, Fat tree encoder stage are designed and integrated. The integrated flash ADC is operated at 3-bit precision with analog input voltage of 0 to 1.8V, supply voltage 3.6V, Resolution 3bits, consumes 24.73mW power, speed is 2.41GS/s. The ADC is designed and implemented in standard gpdk180nm technology of version – IC 6.1 (Higher Version) using Cadence virtuoso tool .The model presented in this paper also can be extended for 90nm,45nm for further processing.

References

[1] J. M. Rabaey, A. Chandrakasan, and B. Nikolic′, “Digital Integrated Circuits”, 2nd Edition, 2003.

[2] E. Säll, "Implementation of Flash Analog-to-Digital Converters in Silicon-On-Insulator Technology," Linköping Studies in Science and Technology, Thesis No. 1213, ISBN 91-85457-79-5, Linköping, Sweden, Dec. 21, 2005.

[3] Maxim Integrated Products, INL/DNL Measurements for High-Speed Analog to-Digital Converters (ADCs).

[4] Rudy J. van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters”, 2nd Edition, 2005.

[5] Shailesh Radhakrishnan, Mingzhen Wang, Chien-In Henry Chen,“Low-Power 4-b 2.5GSPS Pipelined Flash Analog-to-Digital Converters in 3um CMOS”, IEEE Instrumentation and Measurement Technology Conference, vol. 1, pp. 287 – 292, May. 2005.

[6] J. Yoo, "A TIQ Based CMOS Flash A/D Converter for System-on-Chip Applications", PhD Thesis, the Pennsylvania State University, May 2003.

[7] http://interscience.in/IJESS_Vol1Iss_3/paper 10.pdf