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DESIGN OF PULSE-TRIGGERED FLIP-FLOP FOR LOW POWER APPLICATIONS USING BOOST BODY-DRIVEN SCHEME

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ABSTRACT

In this work, Pulse-Triggered Flip-Flop Design for Low Power Applications using Boost Body Driven Scheme is presented. Two techniques, body driven boost and signal feed through schemes has been used in designing this low power flip-flop. Signal feed through scheme helps in faster charging and discharging of output node Q through pass transistor logic. Body driven boost makes faster switching and low power dissipation at intermediate nodes by applying a negative bias scheme at the substrate (or body) terminal of transistors. A modified clock pulse generator is used for better pulse width and height. Simulations have been carried out using CMOS 90nm process technology at 500 MHz clock frequency. All results are optimized for power-delay product with 42.8% saving at 50% switching activities in comparison to conditional pulse enhancement scheme flip flop.

KEYWORDS: Flip-Flops, Low Power, Pulse Triggered, Body-Driven Scheme.

With the scaling of transistors, maintenance of power consumption of VLSI chips has been increasing. Moore's Law drives VLSI technology to continuous enhances in transistor densities and higher clock frequencies. The developments in VLSI technology scaling in the preceding few years reveal that the number of on-chip transistors has been increased by 40% every year. The operating frequency of VLSI systems increases approximately 30% every year. Although capacitances and supply voltages are decreasing meanwhile, a power consumption of the VLSI chips is raising continuously. In contrast, cooling systems cannot improve as rapid as the consumption of power increases. Therefore, in the very close future chips are expected to have limitations of cooling system and solving this problem will be expensive and inefficient.

Flip-flops (FFs) are the most commonly used memory elements for electronic circuits. Many electronic circuits employ several FF-rich modules like register files, shift registers, and first in first out systems (Hwang et al.; 2012). It is figured out that the clock distribution circuits and memory elements are consumed40-45% of the total consumption of power. FFs thus contribute a fairly huge segment of the chip area and consumption of power to the overall system. Pulse-triggered FF (PTFF), because of its single-latch structure, is generally used than the conventional master–slave based FFs and transmission gate FFs in high-speed applications. Apart from the speed advantage, its circuit simplicity reduces the consumption of power of the clock distribution system. A PTFF comprises of a clock pulse generator and a latch for data processing. If the triggering pulses in clock pulse generator are sufficiently narrow, then latch performs like an edge-triggered FF. Pulse generation methods can be categorized as implicit and explicit triggered method (Lin; 2014). In an implicit-type PTFF, the pulse is generated within the flip flop, and no explicit pulse signal yields, but in an explicit-type PTFF, pulse generator and latch are separately utilized.

In this paper, section II describes some implicit and explicit type FFs. Section III explains proposed FF design. Simulations results are shown in next section and then conclusion of this paper.

CONVENTIONAL FLIP-FLOPS

Implicit Pulsed Data Close to Output (ip-DCO) (Tschanz et al.; 2001)

It is implicit type of Pulse triggered flip-flop. It stands for implicit pulsed data close to output is shown in Fig. 1. It comprised of two parts, the first one is pulse generator which is work on the AND logic and second is semi-dynamic latch design which can interface both static and dynamic structure. Implementing logic design is easy and it has less delay. It also occupies small area which is the main advantage of this design. As shown in Fig. 1, the inverters I5 and I6 have been used to latch data and inverter I7 and I8 have been employed to hold the internal node. Clock signal takes the complementary signal with a delay to generate a transparent window equal in size to delay via inverter I1-I3. The main disadvantage of this design is that it has larger switching power and higher capacitance load that affects the speed and degrade the performance.

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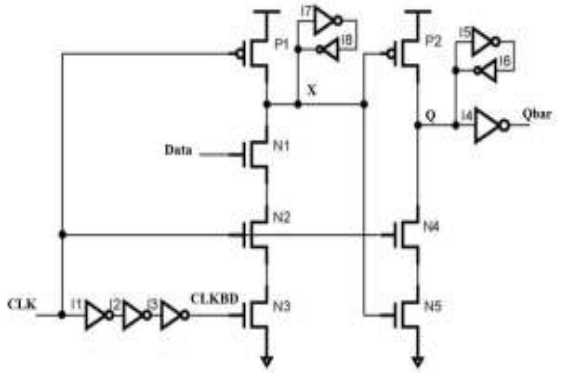

Figure 1: Circuit diagram of ip-DCO PTFF (Tschanz et al.; 2001)

Modified Hybrid Latch Flip Flop (MHLFF) (Rasouli et al.; 2005)

MHLFF stands for modified Hybrid latch flip-flops depicted in Fig.2. It employs static latch structure. In this design, node X is not pre-charge periodically by clock signal. This node X is maintained high because it is controlled by weak pull up transistor P1 which reduce unnecessary discharging. The main disadvantage of this design is during '0' to '1' transistor. There is no longer D to Q delay and the coverage area is high because we require larger transistor to improve the capability of discharging. When both the data and output Q are equivalent to 1 or high there is extra power consumption because of floating node.

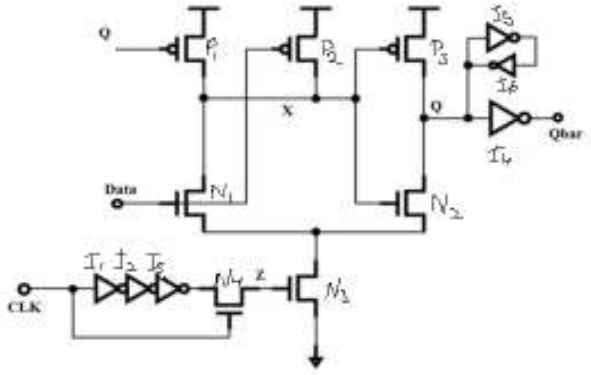

Figure 2: Circuit diagram of MHLFF (Rasouli et al.; 2005)

Single Ended Conditional Capturing Energy Recovery Flip Flop (Mahmoodi et al.; 2009)

SCCER stands for single ended conditional capture energy recovery FF which is shown in Fig. 3. This is implicit type FF design which uses conditional discharge technique. It controls the discharge path by simply eradicating the switching activity when the input is high. The extra NMOS transistor N3 is used in this design and this extra NMOS transistor is control by Qbar which eliminate the unwanted switching activity (if D=1 there is no discharge). In this design, the discharge path includes NMOS transistors N2 and N1 are connected in series.

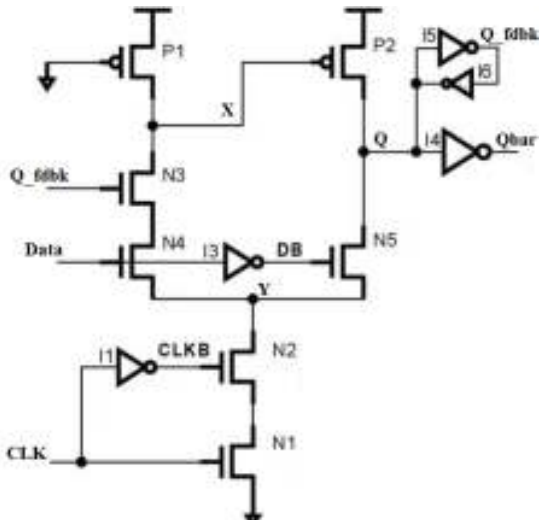

Figure 3: Circuit diagram of SCCER (Mahmoodi et al.; 2009)

Conditional Pulse Enhancement scheme based FF

In the Fig. 4, conditional pulse enhancement scheme based low power FF (Hwang et al.; 2012) design has been presented. Best thing about this FF is that it uses only 4 transistors to generate clock pulse for FF operation. But longest discharging path is formed when input data is at logic "1" while the inverted output Qb is at logic "1". To boost the discharging at this condition, an extra PMOS transistor P3 has been employed at the right side of the top as shown in Fig.4. This PMOS transistor is usually turned off because intermediate node X is almost at logic "1" (high) during operation. At the time of the rising edge of the clock, the clock inverter generate inverted clock output node back to zero but with some delay because upper PMOS transistor is weak. This operation generates the clock pulse which is taller in height, which increases the pull-down strength of lower N6 NMOS transistor that is accountable for the discharging operation. After the clock has been arrive at logic 1, then lower NMOS transistor will turnoff due to zero clock pulse.

After that voltage level of node X becomes high and turns off the P3PMOS transistor. This extra P3 transistor helps in stretching the generated clock pulse

width. It generates clock pulse with adequate width and height for accurate data processing. A massive delay inverter design is no longer required that consumed maximum power in clock generation process. In nutshell, the conditional pulse enhancement technique is effectual save power only when FF output is subject to a data change from logic "0" to logic"1". It also diminishes the leakage power due to lesser size transistors in the discharging path.

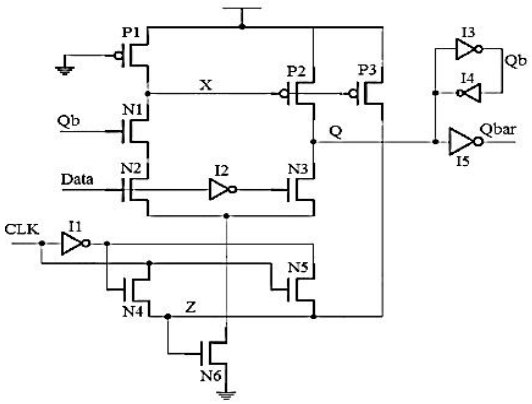

Figure 4: Circuit diagram of conditional pulse enhancement FF (Hwang et al.; 2012)

PROPOSED PTFF DESIGN

Here, to make high performance and low powered flip-flop, conditional pulse enhancement scheme flip-flop (Hwang et al.; 2012) have been changed in four different manners. First, clock pulse generator (modified CLK pulse generator of MHLFF) is changed because of better pulse width and height of CLK pulse (CLKP) which drives three transistors P1, N3 and N8 [6]. CLKP is occurred only at the time of rising edge of the CLK otherwise it remains at logic "0". Second, CLKP is applied in place of permanent ground at the gate of transistor P1 that lowers power dissipation during node X switching. Third, a signal feed through scheme (Lin; 2014) is also applied at output side which directly connects output to input through transistor N3. This scheme helps in faster charging as well as discharging of output node Q through a pass transistor logic. And fourth, to make faster switching and low power dissipation at intermediate node X, a negative bias scheme (Deng and Mo; 2015) is applied at the substrate (or body) terminal of transistor N1 and N2. All these changes make this flip-flop a high performance and low powered flip flop device.

Initially, output Q is supposed to be "0". It makes Qbfb at logic "1".When CLK is "0", then node X charges. If Data is at "1" and CLKP occurs, then node X is discharged via transistors N1, N2 and N8. And it charges output node Q through P2 transistor. But at the same time, a pass transistor N3 is also ON, it helps in charging output node quickly. A negative bias helps in node X discharging faster that generates through transistors N4 and N5 due to high logic at input Data. Data equals to "0", then output discharges through pass transistor N3 at the input Data terminal with the occurrence of CLKP. It means, signal feed through scheme helps in charging and discharging of output Q quickly.

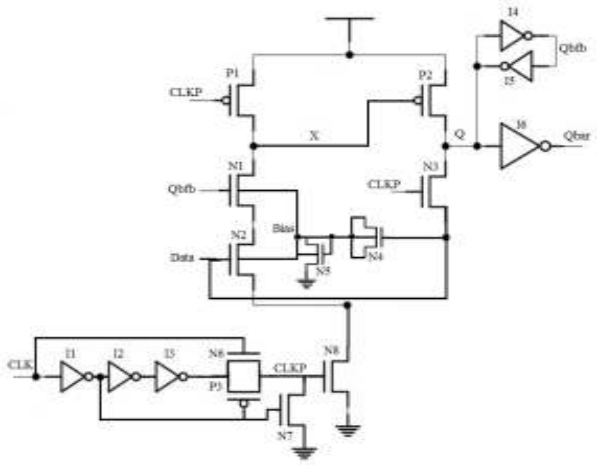

Figure 5: Proposed PTFF Design

SIMULATION RESULTS

To verify the operation of the proposed FF design and the conventional FF designs, simulations are performed using Tanner EDA tool. Simulations are carried out at CMOS 90nm process technology at 1V power supply with 500 MHz clock frequency. All FFs are optimized for power-delay product (PDP) which determines the performance of the particular circuits. A load of 15fF is used at the output of every FFs. In Fig. 6 depicted the simulation output waveforms of proposed design at 100% switching activities. Here, switching activity means that input is switched (or varied) for every clock pulse in 100% activities. It is clearly seen in Table 1 that proposed FF has lower power dissipation, low data-to-Q delay but number of the transistors is higher than conditional pulse enhancement FF. Fig. 7 represents the graphical comparison of FFs at different switching activities with proposed FF.

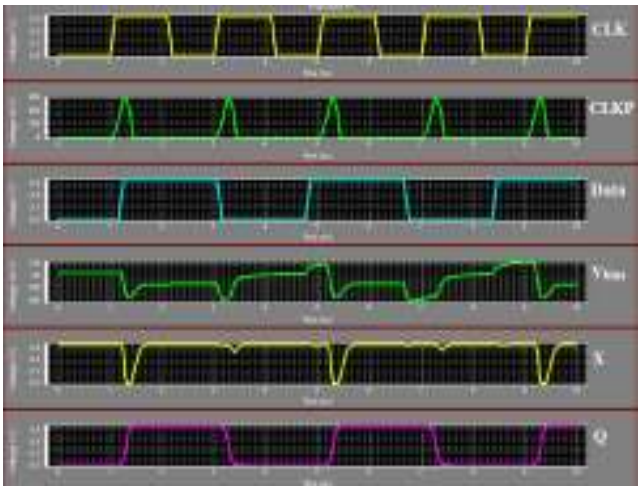

Figure 6: Simulated output waveforms of proposed FF design

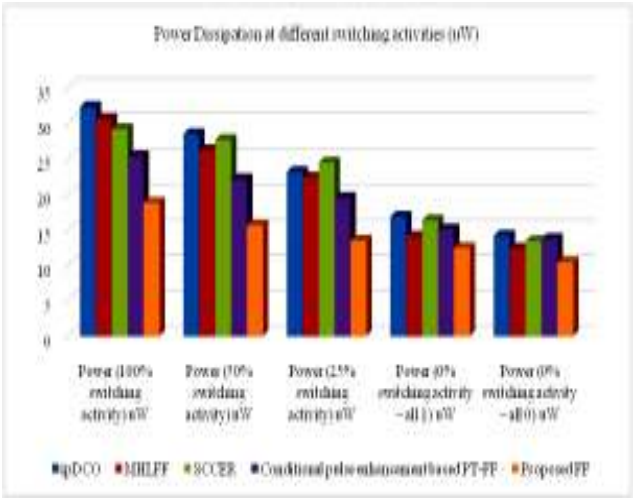

Figure 7: Power dissipation comparison at different switching activities

Table 1: Comparison of different FFs design with proposed FF

Flip –Flops	ipDCO [3]	MHLFF [4]	SCCER [5]	Conditional pulse enhancement based PT-FF [1]	Proposed FF
No. of transistors	23	19	17	19	23
Data-to-Q delay (ps)	131.20	175.43	134.05	123.56	100.22
Power (100% switching activity) uW	32.33	30.64	29.21	25.38	18.82
Power (50% switching activity) uW	28.51	26.23	27.68	22.15	15.64
Power (25% switching activity) uW	23.16	22.37	24.49	19.52	13.47
Power (0% switching activity – all 1) uW	16.86	14.05	16.34	15.09	12.45
Power (0% switching activity – all 0) uW	14.18	12.38	13.41	13.71	10.42
PDP (fJ) at 50% switching activity	3.74	4.60	3.71	2.73	1.56

CONCLUSION

A pulse triggered FF design for low power applications using boost body driven scheme is presented in this paper. Different PTFF are studied for power dissipation and delay performance at CMOS 90nm process technology. Body driven boost and signal feed through scheme make this design low power efficient. Observed results show lowest PDP for proposed FF to make it applicable for various applications. Proposed FF has 42.8% saving of PDP at 50% switching activities in comparison to conditional pulse enhancement scheme flip flop. If we use dual edge triggered clock pulse generator (Kumar et al.; 2016), then same results will be obtained with low power dissipation than single edge triggered FF but it increases no. of transistors.

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