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DESIGN AND ANALYSIS OF NESTED NEUTRAL POINT CLAMPED (NNPC) INVERTER WITH INDUCTIONMOTOR FOR CAPACITOR VOLTAGE-BALANCING METHOD

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Abstract **-** In this paper proposes a capacitor voltage-balancing method for a nested neutral point clamped (NNPC) inverter with induction motor. The NNPC inverter is a newly developed four-level voltagesource inverter for medium-voltage applications. An induction motor is any of a class of rotary electrical machines that converts direct current electrical energy into mechanical energy. A capacitor voltage-balancing method for a nested neutral point clamped (NNPC) inverter is proposed in this paper. To control and balance flying capacitor voltages the proposed capacitor voltage-balancing method takes advantage of redundancy in phase switching states. In this project we are using the induction motor as load due to some advantages. Such as, Speed control over a wide range both above and below the rated speed, High starting torque, Accurate steep less speed with constant torque.The proposed method needs very few computations and also easy to implement. The NNPC inverter is a newly developed four-level voltage source inverter for medium-voltage applications.Small induction motors are used in tools, toys, and appliances. Larger induction motors are used in propulsion of electric vehicles, elevator and hoists, or in drives for steel rolling mills.The proposed method is easy to integrate with different pulse width modulation schemes. By using the simulation results we can analyze the effectiveness and feasibility of the proposed method.

keywords**—** Capacitor voltage-balancing method, multilevel inverter, nested neutral point clamped (NNPC) inverter, Induction motor, voltage source inverter.

I. Introduction

In recent year, Multilevel inverters are extremely famous in medium voltage applications and electrical motor which will reduce the harmonics distrotion, voltage stress on switches will be reduced , low switching frequency and also reduceswitching loss[1]. The multilevel inverters classified into neutral point clamped(NPC) inverter, flying capacitor (FC) inverter, cascaded H-connect inverter, and also the modual multilevel converter [2]– [3]. There are various control techique including capacitor voltage-balancing techniques have been produced in the writing for multilevel inverters [4]. In this paper another multilevel topology is proposed. i.e, nested neutral point clamped (NNPC) inverter appeared in Fig. 1. This topology is a mix of a FC topology with a NPC topology, which gives four levels in output voltage. In correlation with the four-level NPC inverter, the NNPC inverter has less number of diodes, and in contrast with four-level FC inverter, it has less capacitors [6]. All switches in the topology have a similar voltage stretch equivalent to 33% of dc-interface voltage. The NNPC inverter can work in an extensive variety of 2.4– 7.2 kV without the requirement for associating power devices in arrangement.

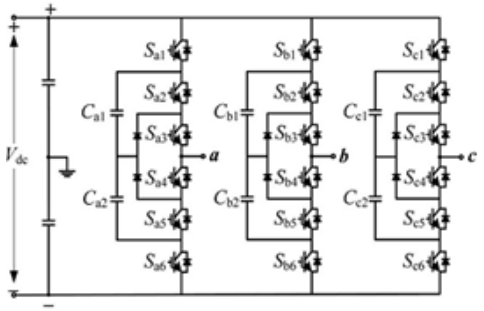

Fig.1. Three phase nested neutral-point clamped (NNPC) inverter.

As can be seen from Fig. 1, the NNPC topology has two FCs in every leg. The voltage over every capacitor ought to be controlled and adjusted at 33% of dc-link voltage (Vdc/3) to guarantee that the inverter can work ordinarily [6]. So as to relieve the previously mentioned disadvantages, another capacitor voltage-adjusting strategy for the NNPC inverter is proposed in this paper. In the proposed technique, basic rationale tables are produced to control the voltages of FCs. The proposed strategy has the accompanying highlights:

1) The strategy is reasonable for and can be effectively incorporated with various pluses width modulation (PWM) plans, for example, SPWM and SVM, and so forth;

2) The technique utilizes basic rationale tables, needs not very many calculations, and is anything but difficult to actualize. The distinction in the topology causes diverse conduct in capacitor voltages and along these lines require distinctive voltage-balancing techniques.

According to the control yield voltage and get FC voltage adjust, a space vector regulation (SVM) method is introduced in [6] for NNPC inverter. In this technique, a cost work is characterized in light of the vitality put away in capacitors. The cost work should be ascertained over and over for each repetitive exchanging state in each testing period to locate the best changing state to adjust FC voltages.

II. Objective

According to the main objective which is represent in this paper is to capacitor voltage-balance technique with the

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combination of nested neutral point clamped (NNPC) inverter is proposed. The NNPC inverter is a recently created four-level voltage source inverter for medium-voltage applications with properties, for example, working over an extensive variety of voltages. The proposed capacitor voltage-balanced technique exploits excess in stage changing states to control which is according to the balanced flying capacitor voltages. Simple and logic tables are created for the adjusting control. Keeping in mind the end goal to control yield voltage and get FC voltage adjust, a space vector modulation (SVM) system is introduced in for NNPC inverter. This technique utilizes basic rationale tables, needs not very many calculations, and is anything but difficult to execute.

III. Problem Definition

In this method, a cost function is defined based on the energy stored in capacitors. The cost function needs to be calculated repeatedly for each redundant switching state in every sampling period to find the best switching state to balance FC voltages. This method is complex and needs lots of calculations due to a large number of redundant switching states and introduces a considerable time delay in the actuation. At a low modulation index (less than 0.5), the number of switching redundancies goes very high, and therefore, the number of calculations will increase significantly. This computational delay can deteriorate the performance of the control system.

IV. Operation Of The Nnpc Inverter And Behavior Analysis Of The Capacitor Voltages

A. Operation of the NNPC Inverter

According to the three-stage NNPC inverter is appeared in Fig. 1. Each phases of inverter will contents of six switches, two FCs , and two clamped diodes . The voltages of the FCs ought to be kept at 33% of dc link voltage (Vdc/3) to create four output levels in stage voltage and guarantee that all the power switches share a similar voltage stress.

according to Table I demonstrates the stage voltagevk (k=a, b, c), yield levelLk, and additionally the comparing stage exchanging stateSk.

For each stage, the four output voltages are −Vdc/2, −Vdc/6, Vdc/6, and Vdc/2, relating to the four output levels 0, 1, 2, and 3, individually. The relationship of vk and Lk which can express below

$$v_k = (2L_k - 3)V_{dc}/6 \qquad (1)$$

As can be seen from Table I, levels 0 and 3 have no repetitive switching state, while levels 1 and 2 both have two excess switching states. The repetitive switching states for level 1 are 1A[001101] and 1B[100110]. The two excess exchanging states create a similar yield voltage−Vdc/6 with distinctive switches ON and OFF. For level 2, the two excess exchanging states are 2A[011001]and 2B[101100], producing a similar stage voltage Vdc/6 with various switches ON and OFF.

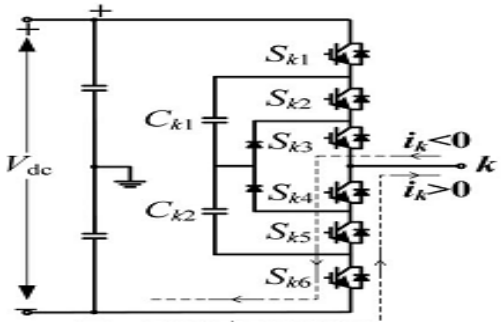
Table I: Phase Voltages And Switching States In NNPC Inverter (K=A, B, C)

Phase voltage,v_k	Output Level,L_k	Phase switching States s_k	Switching states of each device					
			s_{k1}	s_{k2}	s_{k3}	s_{k4}	s_{k5}	s_{k6}
$V_{dc}/2$	3	3	1	1	1	0	0	0
$V_{dc}/6$	2	2A	0	1	1	0	0	1
		2B	1	0	1	1	0	0
$-V_{dc}/6$	1	1A	0	0	1	1	0	1
		1B	1	0	0	1	1	0
$-V_{dc}/2$	0	0	0	0	0	1	1	1

B. Behavior Analysis of the Capacitor Voltages in the NNPC Inverter

There are various switching states impactsly affect FC voltages. The examination of this effect is represented in Fig. 2, in which the six general switching states are estimated.

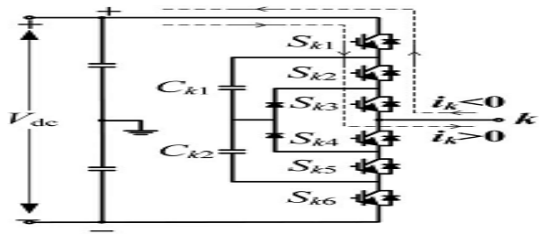
In Fig. 2, Ck1 andCk2 are the two arrangement FCs in the stage k(k=a, b, c), whose voltages are signified byVCk1 andVCk2.



(a) Switching state 0.

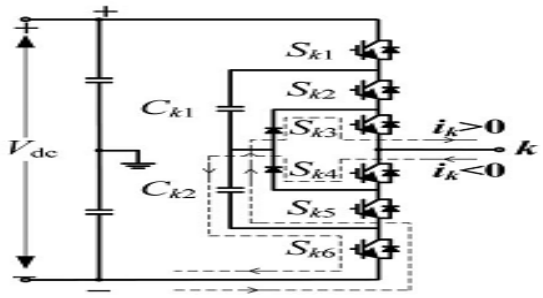
Fig. 2. Impacts of different phase switching states and phase current on capacitor voltages in NNPC inverter

According to the Fig. 2(a) and (f), then the switching states will be 0 and 3 (relating to levels 0 and 3, separately) have no effect on the capacitor voltages because there will be no current flows through the capacitors. .



(f) Switching state 3

According to the Levels 1 and 2 which will dependably have impacts on capacitor voltages. The effects are distinctive for various repetitive switching states and it also based upon the direction of the phases current.

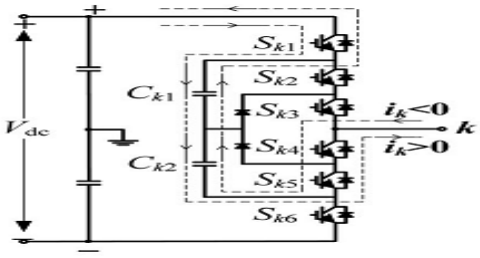


(b) Switching state 1A

Fig. 3. Impacts of different phase switching states and phase current on capacitor voltages in NNPC inverter

As per the level 1, when the redundant switching state 1A is utilized and ik >0, the capacitor Ck2 discharges and VCk2 reduces, and if ik <0, the capacitor Ck2 charges andVCk2 increments, while there is no effect on capacitorCk1,asshown in Fig. 2(b).

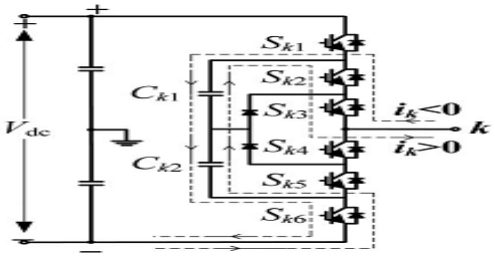
In the event that the state 1B is utilized, both the capacitorCk1 andCk2 charge and capacitor voltage VCk1 andVCk2 increment when ik >0, and both Ck1 andCk2 release andVCk1 andVCk2 diminish when ik <0,as appeared in Fig. 2(c).



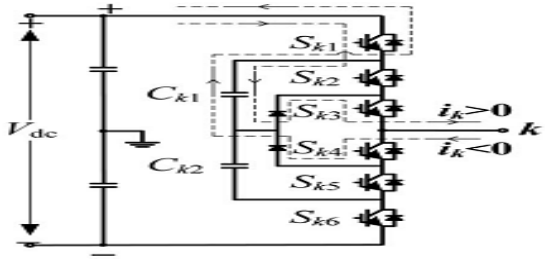
(c) Switching state 1B

Fig. 2. Impacts of different phase switching states and phase current on capacitor voltages in NNPC inverter

According to the estimation which is replaced by the level 2 which is explained in the Fig. 2(d) and (e) according to the redundant switching states 2A and 2B.



(d) Switching state 2A



(e) Switching state 2B

Fig. 2. Impacts of different phase switching states and phase current on capacitor voltages in NNPC inverter. Table II compresses the practices of FC voltages under various switching states and current . As investigated above, levels 0 and 3 have no effect onVCk1 andVCk2, while level 1 (with repetitive switching state 1A and 1B) and level 2 (with excess switching state 2A and 2B) it will affect VCk1 andVCk2 relying upon the switching state and the course of phases current.

IV. Proposed Capacitor Voltage-Balancing Method

A. Algorithm of the Proposed Method

Therefore there will be no control on the voltages of the FCs in the NNPC converter, the FC voltages will be derivatied by the desired output and this is on the grounds that there is no influence over the flow which is represented by in and out from the capacitors. The distinction between the FC voltage and the dersied voltage (Vdc/3) can be characterized as voltage deviation of the FC and can be communicated as

$$\Delta V_{Cki} = V_{Cki} - V_{dc}/3 \qquad (2)$$

Where VCki are the capacitor voltages and ΔVCki are the deviations of the capacitor voltages, k=a, b, c, and i=1,2.

There are various type which are developed by the above principle the two capacitors in an inverter leg are coupled (charged/released mutually) as appeared in Table II.

Table Ii: Behavior Of FC Voltages Under Different Phase Switching States And Phase Currents

Phase voltage,	Output Level,	Phase Current	The behavior of flying capacitor voltages	
v_k	L_k	i_k	V_{ck1}	V_{ck2}
Vdc/2	3	-	No change	No change
Vdc/6	2	> 0	Decrease(2A) Increase(2B)	Decrease(2A), Nochange(2B)
		< 0	Increase(2A) Decrease(2B)	Increase(2A) Nochange(2B)
-Vdc/6	1	> 0	Nochange(1A) Increase(1B)	Decrease(1A), Increase(1B)
		< 0	Nochange(1A) decrease(1B)	Increase(1A) Decrease(1B)
-Vdc/2	0	-	No change	No change

Table III demonstrates the rationale table for controlling capacitor voltageVCk1. The accompanying cases are recorded in the table:

1) If ΔVCk1 <0, then the switching state will be 2A chosen if ik <0; something else, the exchanging state 2B is utilized if ik <0;

2) If ΔVCk1 ≥;0, then theswitching state 2B will be chosen if ik <0; something else, the exchanging state 2A is utilized if ik≥;0.

In this condition, the capacitor voltage VCk1 is totally controllable paying little heed to the bearing of the inverter stage current.

Table III:

Logic Table For Balancing Capacitor Voltage Vck1

Input conditions			Output Results
L_k	ΔV_{ck1}	i_k	The selected switching state(s_k) for controlling V_{ck1}
2	< 0	< 0	2A
		≥ 0	2B
	≥ 0	< 0	2B
		≤ 0	2A

Table IV demonstrates the rationale table for controlling capacitor voltageVCk2. Like Table III, the accompanying cases are recorded:

1) If Δ; VCk2 <0, then the switching state 1A will be chosen if ik <0; something else, the switching state 1B will be if ik ≥;0;

2) If Δ; VCk2 ≥;0, then the switching state 1B will be chosen if ik <0; something else, the switching state 1A will be utilized if ik ≥;0.

Table IV:

Logic Table For Balancing Capacitor Voltage Vck2

Input conditions			Output Results
L_k	ΔV_{ck1}	i_k	The selected switching state(s_k) for controlling V_{ck1}
2	< 0	< 0	1A
		≥ 0	1B
	≥ 0	< 0	1B
		≤ 0	1A

According to the tables which are given in Tables V and VI. For this situation, ΔVCki×ik is utilized as info variable and the rationale is disentangled into two cases for each table. ΔVCki×ik could likewise be supplanted by sign (ΔVCki)×sign(ik)and the administrator "×" could be prepared with operation.

Table V:

Simplified Logic Table For Balancing Capacitor Voltage Vck1

Input conditions			Output Results
L_k	$\Delta V_{ck1} * i_k$		The selected switching state(s_k) for controlling V_{ck1}
2	< 0	< 0	2B
		≥ 0	2A

Table VI

Simplified Logic Table For Balancing Capacitor Voltage Vck2

Input conditions			Output Results
L_k	$\Delta V_{ck1} * i_k$		The selected switching state(s_k) for controlling V_{ck1}
2	< 0	< 0	1B
		≥ 0	1A

B. Integration with Different PWM Schemes

The proposed capacitor voltage-adjusting strategy is appropriate for and can be effectively incorporated with various PWM plans. The schematic outline for reconciliation is appeared in Fig. 3, which could be outlined into the accompanying four stages:

1) First, the yield voltage level Lk can be produced by various PWM plans, for example, SPWM, SVM, and so on.

2) The voltage deviationΔVCk1 andΔVCk2 ought to be computed by (2), and furthermore, the heading of the stage current ik ought to be resolved;

3) Tables V and VI are utilized to decide the best excess changing state out of 1A, 1B and 2A, 2B;

4) Finally, the gating signals are produced and connected to control semiconductors

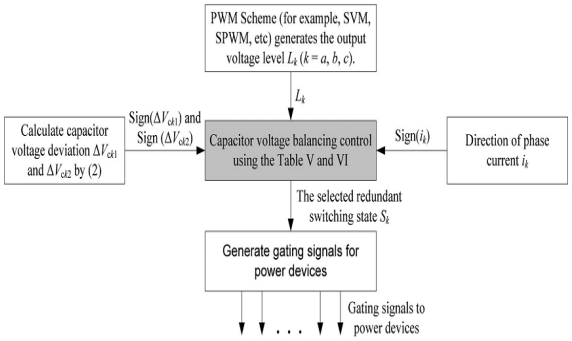


Fig. 3. Schematic diagram for integration of the proposed capacitor voltage-balancing method with PWM schemes.

This technique shows that the proposed capacitor voltage balanced schem, it will be easy, simple and implement will take less time.

V. .Induction Motor

An induction motor (IM) is a type of asynchronous AC motor where power is supplied to the rotating device by means of electromagnetic induction. Other commonly used name is squirrel cage motor due to the fact that the rotor bars with short circuit rings resemble a squirrel cage (hamster wheel).An electric motor converts electrical power to mechanical power in its rotor.

The Induction motor is a three phase AC motor and is the most widely used machine. Its characteristic features are-

- Simple and rugged construction
- Low cost and minimum maintenance
- High reliability and sufficiently high efficiency
- Needs no extra starting motor and need not be synchronized
- An Induction motor has basically two parts – Stator and Rotor

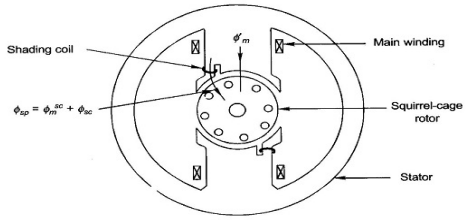


Fig.4. Diagram of induction motor

Principle of operation

When a three-phase supply is connected to the stator windings, a rotating magnetic field is produced. As the magnetic flux cuts a bar on the rotor, an e.m.f. is induced in it and since it is joined, via the end conducting rings, to another bar one pole pitch away, current flows in the bars.

Synchronous Speed:

The speed of the rotating magnetic field is referred to as synchronous speed (NS). Synchronous speed is equal to 120 times the frequency (F), divided by the number of poles (P).

$$.N_s = 120\frac{F}{P} \quad (3)$$

Steady-State Representation

The traditional methods of variable-speed drives are based on the equivalent circuit representation of the motor shown below.

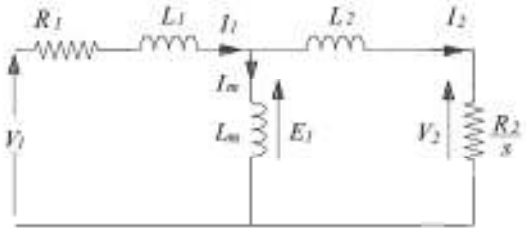


Fig.5.Steady-state equivalent circuit of an induction motor

Power in the rotor circuit,

$$p_2 = 3I_2^2\frac{R_2}{s} = 3V_2I_2 = \frac{3sR_2E_1^2}{R_2^2+(s\omega_1L_2)^2} \quad (4)$$

The output power

$$P_o = P_2 - 3I_2^2R_2 \quad (5)$$

$$= (1-S)P_2 = \omega_0 T \quad (6)$$

$$= \frac{(1-s)\omega_1}{P}T \quad (7)$$

Advantages

The advantages of induction motors are:

1. They are robust and sturdy.

2. They can operate in a wide range of industrial conditions.

3. Induction motors are cheaper in cost. The construction is simple.

4. Induction motors do not have accessories such as brushes, slip rings or commentators

5. Low Maintenance.

6. Very little maintenance is required for induction motors.

7. It does not require any complex circuit for starting.

8. The three phase motor is self starting while the single phase motor can be made self-starting simply by connecting a capacitor in the auxiliary winding.

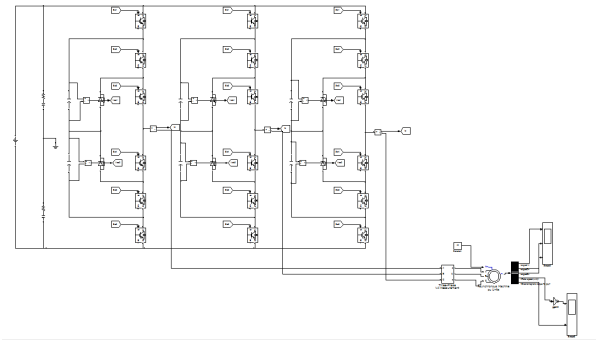


Fig.6.Block diagram of simulation

VI. Simulation Results

As a result of this extended voltage differentiate, armature current will increase and thusly torque and along these lines speed increases. As needs be a induction Motor is prepared for keeping up a comparable speed under factor stack.

Table VII

Simulation Parameters

Simulation parameters	**values**
Output Power	1MVA
Output Voltage	4160V
Flying capacitors	819μF(5.3p.u)
Switching frequency	700HZ
DC Bus voltage	5883v
Fundamental Frequency	60HZ
Load Inductance	24.42mH
Load Resistance	14.65Ω

Modulation index ma used in this paper is given by (3), in which Vref is the given peak phase voltage reference, and Vdc is dc bus voltage

$$m_a = \sqrt{3}V_{ref}/V_{dc} \qquad (8)$$

Two PWM plans, SPWM and SVM, incorporated with the proposed capacitor voltage-adjusting technique, have been examined in both enduring state and transient state.

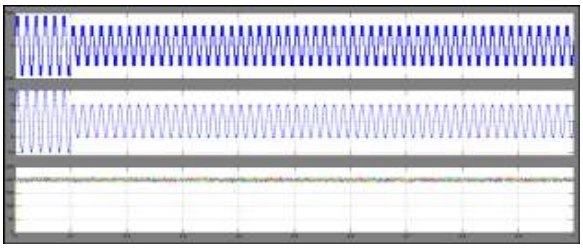


Fig. 7. Simulation results of NNPC inverter with SPWM and the voltage balancing method for ma =0.8 (t<0.1 s) and ma =0.5 (t>0.1 s). (a) Line–line voltage. (b) Phase current. (c) Six FC voltages

Fig. 4 illustrates the simulation results of the NNPC inverter with SPWM and the proposed voltage-balancing method.

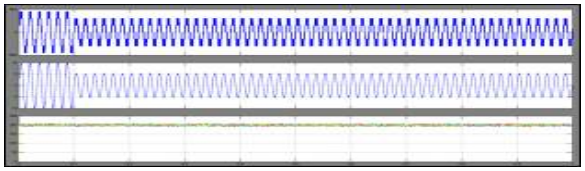


Fig.8. Simulation results of NNPC inverter with SVM and the voltage balancing method for ma =0.8 (t<0.1 s) and ma =0.5 (t>0.1 s). (a) Line–line voltage. (b) Phase current. (c) Six FC voltages.

Fig. 5 demonstrates the reproduction aftereffects of NNPC inverter when SVM and the proposed voltage-adjusting technique are connected, with mama =0.8whent<0.1s, and mama =0.5whent>0.1s.

Dynamic procedures of the FC voltages are additionally researched and appeared in Fig. 6 for SPWM plot and in Fig. 7 for SVM plot with the proposed voltage-adjusting technique.

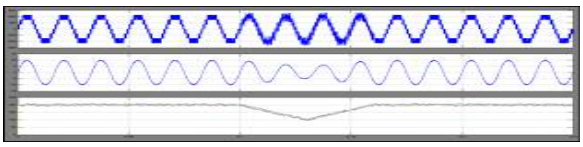


Fig. 9. Simulation results of NNPC inverter with and without the capacitor voltage-balancing control under SPWM scheme. (a) Line–line voltage. (b) Phase current. (c) Six FC voltages.

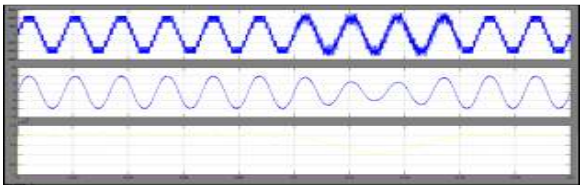
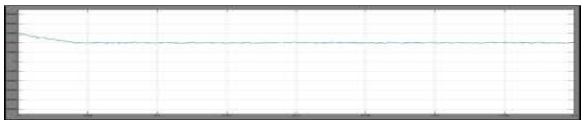


Fig. 10. Simulation results of NNPC inverter with and without the capacitor voltage-balancing control under SVM scheme. (a) Line–line voltage. (b) Phase current. (c) Six FC voltages.

Four distinctive starting capacitor voltage unbalances have been concentrated to confirm the capacity of the voltage-adjusting strategy. The outcomes with m =0.8are appeared in Fig. 11.



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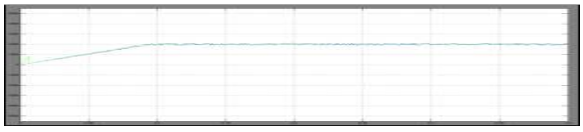

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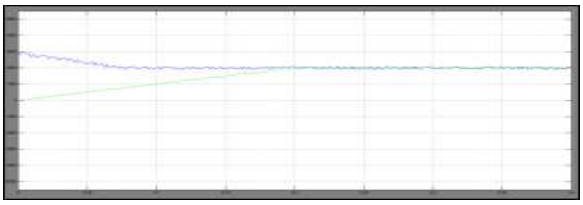
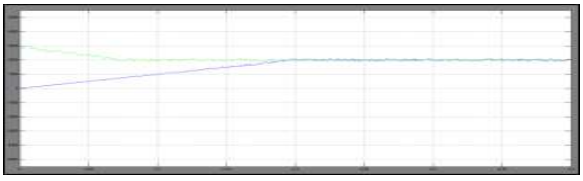


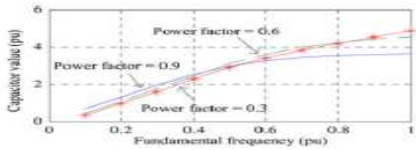
(c)



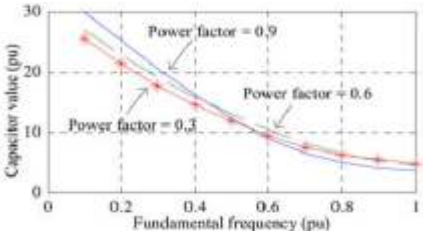
(d)

Fig. 11. Capacitor voltages ofVCa1 andVCa2 starting with different initial voltage unbalances (ma =0.8). (a)VCa1 =VCa2 =Vdc/2.(b)VCa1 = VCa2 =0.(c)VCa1 =Vdc/2andVCa2 =0.(d)VCa1 =0andVCa2 = Vdc/2.

According to the estimation of the two capacitors in a leg of the NNPC inverter are coupled. The coupling will get a few constraints to the inverter a few applications as far as the capacitor estimate.



(a)



(b)

Fig. 12. FC value versus the inverter fundamental frequency with maximum peak-to-peak capacitor voltage ripple of 15%. (a) Fan/pump type of loads. (b) Constant torque type of loads.

Under these conditions, the required capacitor sizes in per unit (p.u.) are given in Fig. 12(a) and (b) for fan/pump and steady torque sorts of burdens, separately.

VII. Conclusion

A capacitor voltage-balance scheme for a nested neutralpoint cinched (NNPC) inverter with induction motor is proposed in this paper. The induction motor has been used in this paper due to some advantages they are robust and sturdy, can operate in a wide range of industrial conditions, Induction motors are cheaper in cost and construction is simple.Induction motors do not have accessories such as brushes, slip rings or commentators .To control and adjust flying capacitor voltages the proposed capacitor voltage-adjusting technique exploits repetition in stage exchanging states. For the control of capacitor adjusting basic and compelling rationale tables are created. The strategy is anything but difficult to actualize and needs not very many calculations. The impediment of the NNPC inverter as far as the voltage adjusting and capacitor measure is additionally examined. In this task we are utilizing the AC engine as load because of a few points of interest. For example, Speed control over a wide range both above and underneath the appraised speed, High beginning torque, Accurate soak less speed with steady torque. The adequacy and attainability of the proposed strategy is controlled by utilizing the reenactment

comes about and furthermore investigate the proposed technique.

References

[1] B. Wu, High-Power Converters and AC Drives.New York, NY, USA: Wiley/IEEE Press, 2006, ch. 1.

[2] N. Mittal, B. Singh, S. P. Singh, R. Dixit, and D. Kumar, "Multilevel inverters: A writing review on topologies and control procedures," in Proc. second Int. Conf. Power, Control Embedded Syst., 2012, pp. 1– 11.

[3] J. Rodriguez, J.- S. Lai, and F. Z. Peng, "Multilevel inverters: A study of topologies, controls, and applications,"IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724– 738, Aug. 2002.

[4] R. Stala, "A characteristic dc-interface voltage adjusting of diode-cinched inverters in parallel systems,"IEEE Trans. Ind. Electron., vol. 60, no. 11, pp. 5008– 5018, Nov. 2013.

[5] J. Mei, K. Shen, B. Xiao, L. M. Tolbert, and J. Zheng, "another specific circle predisposition mapping stage manner PWM with dynamic voltage adjust capacity for particular multilevel converter,"IEEE Trans. Ind. Electron., vol. 61, no. 2, pp. 798– 807, Feb. 2014.

[6] M. Narimani, B. Wu, Z. Cheng, and N. Zargari, "another settled unbiased point cinched (NNPC) converter for medium-voltage (MV) control conversion,"IEEE Trans. Power Electron., vol. 29, no. 12, pp. 5259– 5270, Dec. 2014.

[7] A. Choudhury, P. Pillay, and S. S. Williamson, "DC-connect voltage adjusting for a three-level electric vehicle footing inverter utilizing a creative exchanging succession control scheme,"IEEE Trans. Emerg. Sel. Themes Power Electron., vol. 2, no. 2, pp. 296– 307, Jun. 2014.

[8] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM With dc-connect capacitor voltage adjusting control for diode-clasped multilevel converter based STATCOM,"IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1884– 1896, May 2013.

[9] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage adjusting control of diode-braced multilevel converters with latent front-ends,"IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1751– 1758, Jul. 2008.

[10] S. Busquets-Monge, R. Maheshwari, and S. Munk-Nielsen, "Overmodulation of n-Level three-leg dc-air conditioning diode-braced converters with complete capacitor voltage balance,"IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1872– 1883, May 2013.

[11] A. H. Bhat and N. Langer, "Capacitor voltage adjusting of three-stage unbiased point-braced rectifier utilizing altered reference vector, "IEEE Trans. Power Electron., vol. 29, no. 2, pp. 561– 568, Feb. 2014.

[12] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-adjust restrains in four level diode-cinched converters with aloof front closures, "IEEE Trans. Ind. Electron., vol. 52, no. 1, pp. 190– 196, Feb. 2005.

[13] P. Chaturvedi, S. Jain, and P. Agarwal, "Bearer based unbiased point potential controller with decreased exchanging misfortunes for three-level diode-cinched inverter," IEEE Trans. Ind. Electron., vol. 61, no. 2, pp. 613– 624, Feb. 2014.

[14] M. Khazraei, H. Sepahvand, K. Corzine, and M. Ferdowsi, "A summed up capacitor voltage adjusting plan for flying capacitor multilevel converters," in Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo., 2010, pp. 58– 62.

[15] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Dynamic capacitor voltage adjusting in single-stage flying-capacitor multilevel power converters, "IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 769– 778, Feb. 2012.