FUZZYBASED HIGH STEP-UP DC TO DC CONVERTER WITH FUEL CELL POWER SYSTEM UNDER ALTERNATING PHASE SHIFT CONTROL

[1]Saleem Mohammad, [2]CH.Shashidhar, [3]Manoj Nethala

[1]Electrical and Electronics Engineering, Sathyabhama Institute of science & Technology, Chennai
[2]Department of Electrical and Electronics Engineering, Veltech Rangarajan Dr Sagunthala R &D Institute of Science and Technology, Chennai
[3]Department of Electrical and Electronics Engineering, Aurora's Scientific Tech& Research Academy, Hyderabad

Abstract: In this project we are implementing a new pulse width modulation (PWM) technique, which is combination of alternating phase shift (APS) control and traditional interleaving PWM control for the two-phase interleaved boost converter with voltage multiplier for fuel cell power system. Fuzzy controller is denoted as human decision making mechanism which provided the operation for the electronic system with the expert decision. According to the APS control which is utilized for the better performance in case of heavy load. Therefore the boundary condition for swapping between traditional interleaving PWM control and APS control which is derived. According to the analysis, we get the combination of APS control and traditional interleaving control which is denoted as full power range control which have been proposed. Moreover to explore the efficiency of the converter this is given by analysis the Loss breakdown. And finally we can verify by using simulation.

Keywords—Boost converter, fuel cell, interleaved, loss breakdown, and voltage multiplier.

I. Introduction

Fuel cell is one of promising decisions because of its favorable circumstances of zero emission, low noise, higher power density and being effortlessly modularized for versatile power sources, electric vehicles, distributed generation systems and so on [1].

The grid-connected power system based on fuel cell is shown in Fig. 1. For a common 10-kW proton trade film energy unit, the yield voltage is from 65 to 107 V. A high advance up dc/dc converter is required for the framework as appeared in Fig. 1. The dc/dc converter will produce a high recurrence input current swell, which will lessen the life time of the power device stack [2]– [4]. Thusly, the dc/dc converter for the system as appeared in Fig. 1 should have high step-up ratio with minimum input current ripple
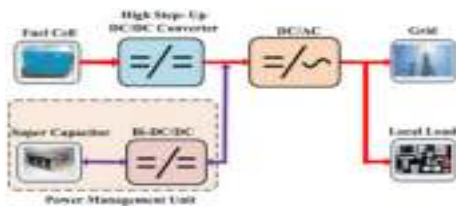

Fig. 1. Grid-connected power system based on fuel cell.

High step-up ratio can be achieved by combining classical boost converter with switched inductors [6], coupled inductors [7]–[9], high-frequency transformer [10], or switched capacitor [11]. They can acquire high advance up proportion with high productivity, low-voltage stress, and low electromagnetic interference. To overcome the decreases the output fuel cell struck current ripple or the dc/dc converter input current ripple according to the

passive filter or dynamic channel [5] can be utilized, in any case, this will expand the unpredictability of the system. According to the interleaving the dc/dc converter can decrease the input current ripple of the dc/dc converter. An interleaved boost converter with voltage multiplier was proposed. The interleaving support converter with voltage multipliers is appeared in Fig. 2.
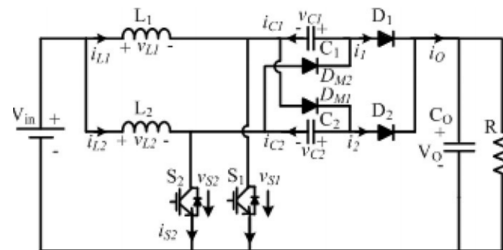

Fig. 2. Structure of two-phase interleaved boost converter with voltage multiplier

The converter appeared in Fig. 2 which can be attached to the low-voltage stress in the power device, which builds the change efficiency. According to the heavy load and the voltage stress according to the power devices which May increases which will be implemented in DCM mode, which happens when energy component just supplies a light neighborhood stack as appeared in Fig. 1. For this situation, higher voltage control system should be utilized, and along these lines its cost and power loss will be expanded. According to the new pulse width modulation (PWM) control method, named as alternating phase shift (APS), to enhanced the problem whenever the converter is operated in the light load

II. Objective

The main objective of this paper is to reduce the voltage stress and also to achieve the better performance in heavy load .therefore in order to overcome this we are implementing a novel PWM method with the two phase interleaved boost converter and voltage multiplier with the fuel cell by the combination of APS and the traditional interleaving PWM control. Therefore according to the APS control is used to reduce the voltage stress on switches in light load while the traditional interleaving control is used to keep better performance in heavy load. . Loss breakdown analysis is also given to explore the efficiency of the converter.

III. Problem Definition

In this paper we have to overcome the problem such as voltage stress , current and voltage ripple and power loss therefore to overcome this we are implementing the novel PWM scheme for two-phase interleaved boost converter with voltage multiplier for fuel cell power system by combining APS and traditional interleaving PWM control. By utilizing APS control is used to reduce the voltage stress on switches in light load while the traditional interleaving control is used to keep better performance in heavy load. Interleaving the dc/dc converter can reduce the input current ripple of the dc/dc converter. a new pulse width modulation (PWM) control method, named as alternating phase shift (APS), to overcome the problem when the converter operates in light load.

IV. Literature Survey

G. Fontes, C. Turpin, S. Astier, and T. A. Meynard: This paper proposes a theoretical and experimental study of the behavior of a fuel cell stack subject to current harmonics. The fundamental role of the internal double layer capacitor is demonstrated [1].

P. Thounthong, B. Davat, S. Rael, and P. Sethakul: Fuel starvation is defined as the failure of the fuel system to supply sufficient fuel to allow the engine to run properly, for example due to blockage, vapor lock, contamination by water, malfunction of the fuel pump or incorrect operation, leading to loss of power or engine stoppage.[2]

Wang, Y. Kenarangui, and B. Fahim: In this paper results obtained from analysis and design of a soft-switching boost converter for a fuel-cell-system is discussed. It is demonstrated that by utilizing ZVS and ZCS techniques, high-frequency/high-power density converters can be designed to match the high power density of fuel cells. Current ripple limitation of fuel cells is discussed in this paper [3].

S. K. Mazumder, R. K. Burra, and K. Acharya: We describe an energy-efficient, fuel-cell power-conditioning system (PCS) for stationary application, which reduces the variations in the current drawn from the fuel-cell stack and can potentially meet the $40/kW cost target. The PCS consists of a zero-ripple boost converter (ZRBC) followed by a soft-switched and multilevel high-frequency (HF) inverter and a single-phase cycloconverter. The ZRBC comprises a new zero-ripple filter (ZRF), which significantly reduces the input low- and high-frequency current ripples,thereby potentially enhancing the durability of the stack[4].

B. Axelrod, Y. Berkovich, and A. Ioinovici,: The proposed hybrid converters contain the same number of elements as the quadratic converters. The superiority of the new, hybrid converters is mainly based on less energy in the magnetic field, leading to saving in the size and cost of the inductors, and less current stresses in the switching elements, leading to smaller conduction losses[5].

Z. Qun and F. C. Lee,: The proposed converters, which use diodes and coupled windings instead of active switches to realize functions similar to those of active clamps, perform better than their active-clamp counterparts. High efficiency is achieved because the leakage energy is recycled and the output rectifier reverse-recovery problem is alleviated[6].

L. Wuhua, F. Lingli, Z. Yi, H. Xiangning, X. Dewei, and W. Bin,: The proposed system includes a high-efficiency high-step-up interleaved soft-switching flyback-forward converter and a full-bridge inverter. Therefore, high-efficiency and high-power-density conversion can be achieved in a wide input-voltage range by employing the proposed system[7].

Y. Changwoo, K. Joongeun, and C. Sewan,: multiphase dc-dc converters are proposed for high-voltage and high-power applications. the proposed converter has the following features: high-step-up voltage gain with significantly reduced transformer turn ratio, low-input current ripple due to interleaving effect, zero-voltage switching turn-ON of switches flexibility in device selection resulting in optimized design[8].
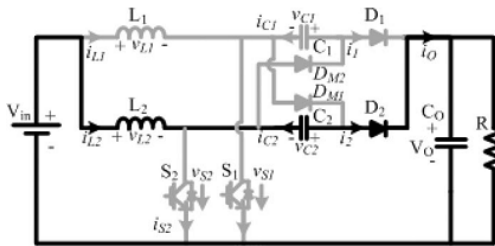
R. D. Middlebrook,:A novel switching DC-to-DC converter is introduced in which large voltage step-down ratios can be achieved without a very small duty ratio and without a transformer. The circuit is an extension of the Cuk converter to incorporate a multistage capacitor divider[9].

A. A. Fardoun and E. H. Ismail,: In this paper, a new single-switch no isolated dc-dc converter with high voltage transfer gain and reduced semiconductor voltage stress is proposed. In addition, the low voltage stress across the diodes allows the use of Scotty rectifiers for alleviating the reverse-recovery current problem, leading to a further reduction in the switching, and conduction losses[10].

V. Boundary Condition Analysis With Traditional Interleaving Control For Low Power Operation

According to the components in the converter which are perfect, both capacitor C1 and C2 are sufficiently enough, and duty cycle is under 0.5. The operation of an switching cycle of the converter can be separated into six phases at limit condition which the voltage stress of the power switch will be bigger than half of the output voltage with conventional interleaving control, as appeared in Fig. 3. Regular hypothetical waveforms at limit condition are appeared in Fig. 4.

First Stage(t0,t1): lets as consider that the t0, both switch S1 and S2 are off, the energy is stored inductor L2 and capacitor C2 in past stage are exchanged to the yield capacitor CO through D2 as appeared in Fig. 3(a).

(a)

Fig. 3. Stages at boundary condition.(a) First stage (t0, t1),

Second Stage(t1,t2): lets as t1, the switch S1 is turned ON, the inductor L1 begins to store the energy in the zero as appeared in Fig. 3(b). Meanwhile, if (VC 1 + VC 2) < VO , where VC 1 is the capacitor C1 voltage, the diode D2 will be killed and the diode DM 2 will be turned ON; in this manner, the vitality in the inductor L2 will be exchanged to the capacitor C1.

(b)

(c)

Fig. 3. Stages at boundary condition (b) second stage (t1, t2), (c) third stage (t2, t3),
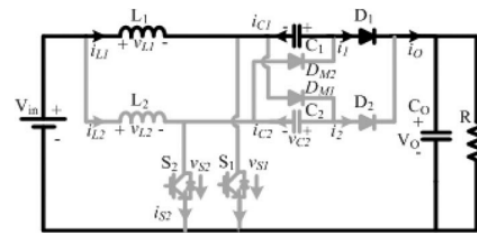
Third Stage(t2,t3): lets as consider the t2, the current in the inductor L2 just tumbles to zero, every one of the diodes are in off state and the inductor L1 is in charging state until the turn S1 is killed right now of t3. The voltage weight on switch S2 is Vin. Toward the finish of this stage, the current in the inductor L1 goes to the pinnacle esteem IL1P , and

$$I_{L1P} = \frac{V_{in} D_m T_S}{L} \quad (1)$$

where Vin is the info voltage, L is the inductance of L1 and L2,Dm is the obligation cycle at limit condition, and TS is the exchanging time frame.

Fourth Stage (t3,t4): lets as consider the t3, switch S1 and S2 are in off express, the vitality in the inductor L1 and the capacitor C1 will be exchanged to the yield capacitor CO through the diode D1, which is like First Stage. In this stage, the voltage weight on switch S1 is (VO − VC 1), and the voltage weight on switch S2 is Vin. Toward the finish of this stage, the current in the inductor L1 reductions to be IL1M

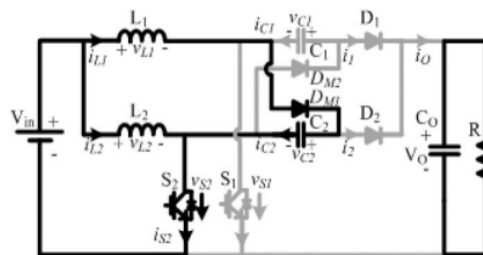$$I_{L1M} = I_{L1P} - \frac{V_O - V_{C1} - V_{in}}{L}(0.5 - D_m)T_s \quad (2)$$

(d)

Fig. 3. Stages at boundary condition (d) fourth stage (t3, t4)

Fifth Stage (t4,t5): lets as consider t4, the switch S2 is turned ON and the inductor L2 begins to store vitality. Toward the finish of this stage, the current in the inductor L1 abatements to zero from IL1M . Furthermore, subsequently
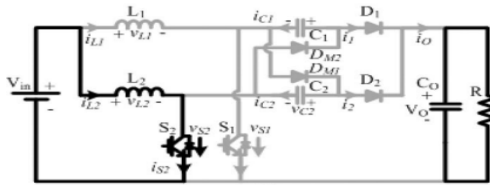
$$I_{L1M} - \frac{V_{C2} - V_{in}}{L}(D_2 - 0.5 + D_m)T_s = 0 \quad (4)$$

where D2 is the duty cycle as shown in Fig. 4.

(e)

Fig. 3. Stages at boundary condition (e) fifth stage (t4, t5),

sixth Stage (t5,t6): lets as consider t5, the current in the inductor L1 abatements to zero. Every one of the diodes are in off state and the inductor L2 is in charging state until the point when the stage reaches the end right now t6. On the off chance that it is not as much as VO , the voltage weight on switch S1 and S2 will be bigger than VO/2, in light of the fact that the voltage weight on switch S1 is (VO − VC 1) amid the Fourth Stage and the voltage weight on switch S2 is (VO − VC 2) amid the First Stage.

(f)

Fig. 3. Stages at boundary condition (f) sixth stage (t5, t6).

The average value of the output current iO is equal to the dc component of the load current VO/R, then

$$\frac{V_O}{R} = \frac{1}{T_S}\int_0^{T_S} i_o dt = \frac{1}{T_S}\int_0^{T_S}(i_1 + i_2)dt = \frac{1}{T_S}\int_0^{T_S} i_1 dt = \frac{1}{T_S}\int_0^{T_S} i_2 dt \qquad (5)$$

Considering the same parameters of the circuit in two phases as shown in Fig. 2, therefore

$$\frac{1}{T_S}\int_0^{T_S} i_1 dt = \frac{1}{T_S}\int_0^{T_S} i_2 dt \qquad (6)$$

By combining (4) and (5), it is derived

$$\frac{V_O}{R} = \frac{2}{T_S}\int_0^{T_S} i_1 dt = \frac{2}{T_S}\int_{t_3}^{t_4} i_1 dt$$

$$= \frac{2}{T_S}\left[\frac{1}{2}(I_{L1P} + I_{L1M})(0.5 - D_m)T_S\right] = ((I_{L1P} + I_{L1M})(0.5 - D_m)) \qquad (7)$$
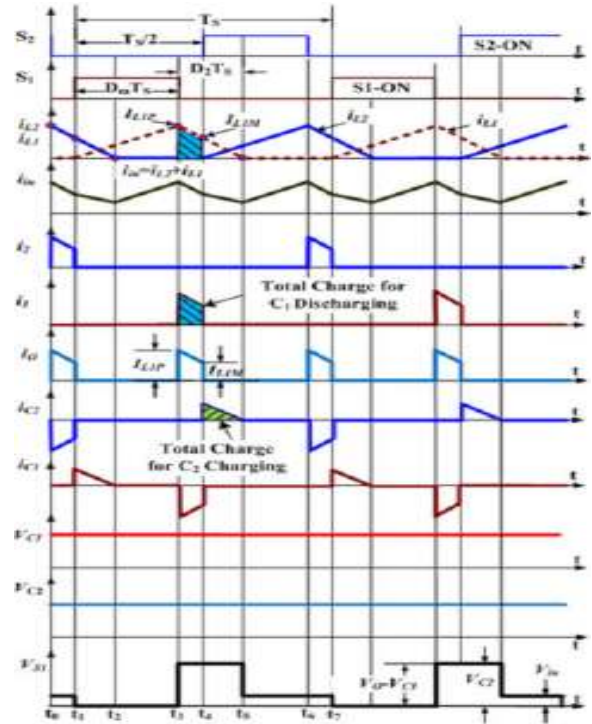
where R is the load.

Fig. 4. Main theoretical waveforms at boundary condition.

At the boundary condition, the diode D2 (D1) approaches the conduction state during the Second Stage (Fifth Stage), which is shown in Fig. 5.
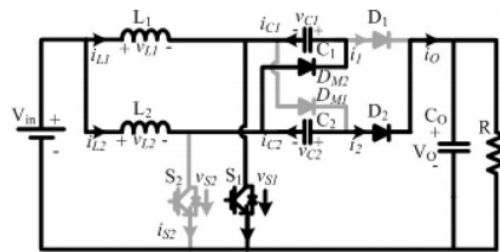

Fig. 5. One stage above boundary condition.

The following equation can be obtained

$$V_{C1} + V_{C2} = V_O \qquad (8)$$

Considering both capacitors C1 and C2 are large enough, average voltage of the capacitor will keep equal. Otherwise, theconverter will not operate at boundary condition, therefore

$$V_{C1} = V_{C2} = \frac{1}{2}V_o \qquad (9)$$

By substituting (1) and (8) into (2), the current IL1M can be derived

$$I_{L1M} = \frac{V_{in} - {V_O}/{2} + V_O \cdot D_m}{2L}T_S \qquad (10)$$

As shown in Fig. 4, the total discharge of capacitor C1 between t3 and t4 is

$$Q_{C1} = \int_{t_3}^{t_4} i_{L1} dt = \frac{1}{2}(I_{L1P} + I_{L1M})(0.5 - D_m)T_S \quad (11)$$

The total charge of capacitor C2 between t4 and t5 is

$$Q_{C2} = \int_{t_4}^{t_5} i_{L1} dt = \frac{1}{2}I_{L1M}(D_2 - 0.5 + D_m)T_S \quad (12)$$

According to the previous analysis, the total discharge of C1 is equal to the total charge of capacitor C2 at boundary condition. Therefore, there will be

$$Q_{C1} = Q_{C2} \quad (13)$$

By combining (10), (11), and (12), the following can be derived

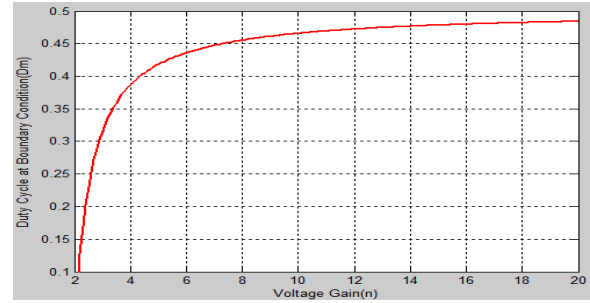$$D_2 = (0.5 - D_m)\left(\frac{I_{L1P}}{I_{L1M}} + 2\right) \quad (14)$$

By combining (3) and (6) and then substituting (1), (9), and (13) into them, the boundary condition can be derived as

$$\begin{cases} K = Kcrit = \frac{n-2}{2n(n-\sqrt{2})^2} \\ D_m = \frac{n-2}{2(n-\sqrt{2})} \end{cases} \quad (15)$$

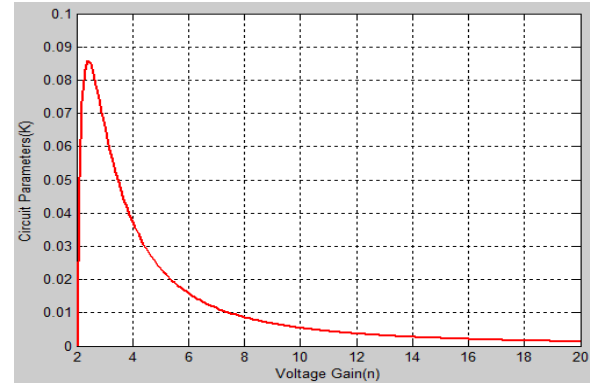where n is the voltage gain of the converter (n = VO/Vin), and K is the parameters of the circuit and K = 2L/(R × TS).

The boundary conditional with conventional interleaving control chose by (14) is appeared in Fig. 6. The requirement incorporates two sections: duty cycle D and the circuit parameters K = 2L/(R × TS).

As the switching period frame TS and the information inductor L are planned at normal operation in consistent conduction mode (CCM), the limitation is dictated by obligation cycle D and the heap R. The motivation behind why there are two sections in the limit limitation is that the duty cycle D changes with the heap when the converter works in DCM. For a given application, the voltage pick up of the dc/dc converter is resolved. And after that, the base duty cycle that can keep up low-voltage stress in primary power gadgets with customary interleaving control will be given by (14)- (b) and as appeared in Fig. 6(a). At a similar least duty cycle, the converter works at limit condition when the circuit parameters K = 2L/(R × TS) fulfill (14)- (an) and as appeared in Fig. 6(b).

(a)

(b)

Fig. 6. Boundary constraint varies with voltage gain. (a) Duty cycle at boundary condition varies with voltage gain, (b) circuit parameters at boundary condition varies with voltage gain.

At the point when the converter works over the boundary condition, the circuit parameters are in Zone A of Fig. 6(b), i.e.,K>Kcrit, the converter could accomplish divided voltage stress on the power switches with traditional interleaving control with the duty cycle over the strong red line as appeared in Fig. 6(a). While reduce the loads from the soild red line at limit condition in Fig. 6(b), i.e., K = Kcrit, the duty cycle of the converter will be diminished to the strong red line in Fig. 6(a). While diminishing the load promote in Zone B in Fig. 6(b), i.e., K <Kcrit, the obligation cycle will be diminished further to be littler than the base duty cycle that keeps up low-voltage weight on switches with conventional interleaving control. At that point, the APS control ought to be utilized to accomplish split voltage stress on the power switches in Zone B [17], [18].

In our 1-kW model plan, the info voltage of the converter is 86– 107 V, and the output voltage of the converter is 700 V. The voltage pick up will differ from n1 = 6.54 to n2 = 8.14, and afterward the circuit parameters at limit conditions Kcrit will fluctuate from Kcrit1 = 0.013 to Kcrit2 = 0.0083 as appeared in Fig. 6(b), the duty cyclewill shift from Dm1 = 0.443 to D m2 = 0.456 with a specific end goal to keep up the steady output voltage.

At the point when the circuit parameters K = $2L/(R \times TS)$ are beneath the strong red line from indicate a point b at various voltage pick up as appeared in Fig. 6(b), the duty cycle will be diminished further to be not as much as the strong red line from D m1 = 0.443 to Dm2 = 0.456 as appeared in Fig. 6(a), and after that the voltage weight on switches will be expanded at this heap. Keeping in mind the end goal to accomplish the divided voltage wstress on the power system switches at this heap, APS control is required.

VI. Control Scheme Of All Power Range With Aps And Traditional Interleaving Control

As indicated by the guideline of APS [17], APS control which is proposed for the light load issue with obligation cycle under 0.5 as appeared in Fig. 7(a). With the load increases the duty cycle will be expanded also. At the point when the obligation cycle is expanded to 0.5, the APS control will be changed to be conventional interleaving control with divided exchanging recurrence as appeared in Fig. 7(b). As indicated by past investigation as appeared in Fig. 6, the base obligation cycle to accomplish low-voltage weight on switches with conventional interleaving control is under 0.5.
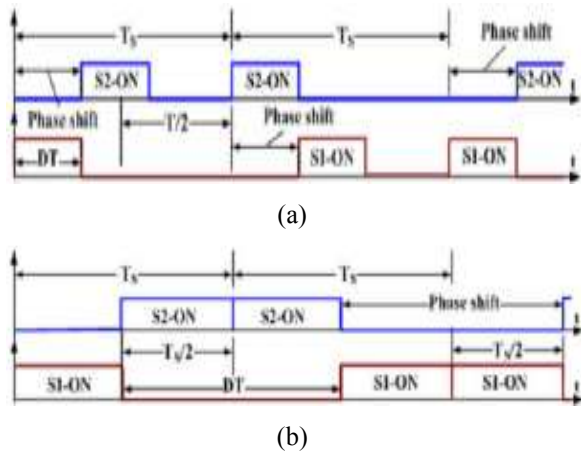

(a)

(b)

Fig. 7. PWM waveform of APS with D < 0.5 and D = 0.5. (a) D < 0.5, (b) D = 0.5.

Considering the variety of the information voltage from 86 to 107 V for 1-kW power device operation and the volatge voltage of the converter 700 V, the minimum duty cycle of traditional interleaving control shifts from Dm1 = 0.443 to Dm2 = 0.456. The control plot is appeared in Fig. 8. The obligation cycle is separated into three territories: D < Dm1,D> Dm2, and Dm1 ≤ D ≤ Dm2. In the second range, i.e., D > Dm2, traditionalinterleaving control will be utilized.

In the principal region (D < Dm1) with APS control and the second zone (D > Dm2) with traditional interleaving control, the capacitor voltage is half of the output voltage.

In this way, the switches voltage stress is clamped to half of the output voltage [17], [18].
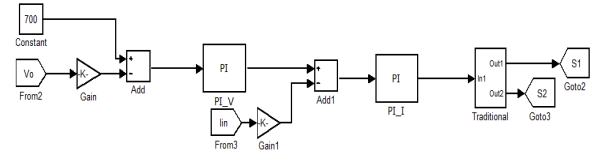

Fig. 8. Block diagram of the converter with the control scheme of all power range

The swapping between the APS control and traditional interleaving control in the territory Dm1 ≤ D ≤ Dm2 is accomplished by distinguishing the voltage worry of the switch S1 as appeared in Fig. 8. On the off chance that the conventional interleaving control is at first utilized as a part of the second region (Dm1 ≤ D ≤ Dm2) and once the switch S1 voltage push is bigger than half of the yield voltage, the rationale unit yield CMP in Fig. 8 will be changed to CMP = 1 and APS control will be empowered. The previously mentioned work for swapping between the APS and customary interleaving control is accomplished by the Logic Unit as appeared in Fig. 8, and the operational guideline of the Logic Unit is appeared in Table I.

Table I :Operational Principle Of The Logic Unit In Fig. 8

v_{s1} > $0.5v_0$	D_{ref} > D_{m1}	D_{ref} < D_{m2}	Control method
X	1	0	Traditional interleaving control
X	0	1	APS control
0	1	1	Keep the previous control mode
1	1	1	Swap from traditional interleaving control to APS control and stay in APS control until $D_{ref} > D_{m2}$

In case APS control mode is utilized (i.e., CMP = 1), the optocoupler transistor T1 is turned ON, the voltage of capacitor C in the pinnacle finder unit is resetted and the pinnacle indicator unit is disenabled. On the off chance that the conventional interleaving control mode is utilized (i.e., CMP = 0), the optocoupler transistor T1 will be killed, and the pinnacle indicator unit is empowered and used to identify the voltage worry of switch S1.

With a specific end goal to accomplish better unique execution operation, double circle control is received as appeared in Fig. 8, in which the inward current circle is to control the information inductor current while the external voltage circle is to control the yield voltage.

Kip and Kii are the PI controller parameters of the internal current circle, while K vp and Kvi are the PI controller parameters of the external voltage circle.

VII. Loss Breakdown Analysis

As the cost of fuel cell is still high, it is imperative to augment the effectiveness of the power converter for fuel cell-based power system in order to overcome the operation cost and increment the usage of energizes. In this manner, misfortune breakdown examination is required. The normal energy of the converter is 1 kW for loss breakdown investigation and model setup, and the information voltage is 100 V while the yield voltage is 700 V with exchanging recurrence fS = 10 kHz. The power system utilized are indicated inTable II.

Table II Main Choices Of Power Devices

symbol	Voltage stress
S_1, S_2	350v
D_1, D_2	350v
D_{M1}, D_{M2}	700v

The converter could work in CCM at ostensible load with input current swell proportion r = 0.37 and the inductor L1 and L2 is 1158 μH. The inductor is worked with the undefined center. As appeared in Fig. 9, the primary parts of the misfortune are the conduction loss (Pcon S) and exchanging misfortune (PSW S) of the IGBT. With the quick recuperation diodes .the proficiency of the converter at ostensible load can be 97.49%.

The converter could likewise work in limit conduction mode (BCM) at ostensible load with input current swell proportion (r = 0.6) and the inductor L1 and L2 is 714.3 μH. The inductor is worked with the formless center. As appeared in Fig. 10, the fundamental parts of the loss likewise incorporate the conduction loss (Pcon S) of the IGBT. Contrasted and CCM as appeared in Fig. 9, there is no quick recuperation loss even with quick recuperation diodes in BCM. Notwithstanding, the inductor loss including the center loss (P Fe) and the wire loss.
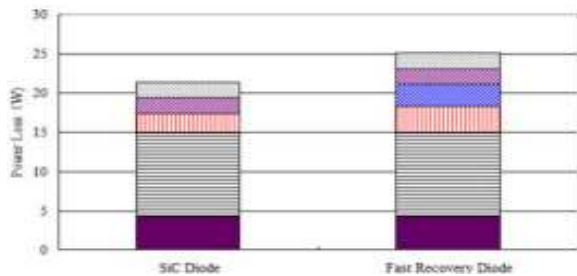

Fig. 9. Loss distribution of the converter with IGBT in CCM with fast recovery diode
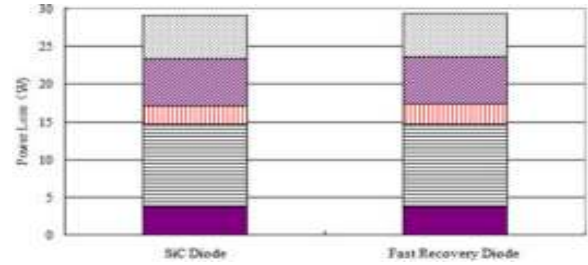

Fig. 10. Loss distribution of the converter with IGBT in BCM with fast recovery diode

In BCM, the productivity of the converter can be 97.09% with SiC diode and 97.06% with quick recuperation diode. Contrasting Fig. 9 and Fig. 10, the productivity of the converter with IGBT and quick recuperation diode in CCM is somewhat higher than that in BCM. In CCM, the effectiveness of the converter with quick recuperation diode is just 0.37% not as much as that with SiC diode. Along these lines, we utilize IGBT and quick recuperation diode in CCM for reenactments.

VIII. Fuzzy Logic Controller

In FLC, essential control activity is dictated by an arrangement of semantic standards. These tenets are controlled by the framework. Since the numerical factors are changed over into phonetic factors, scientific displaying of the framework isn't required in FC.
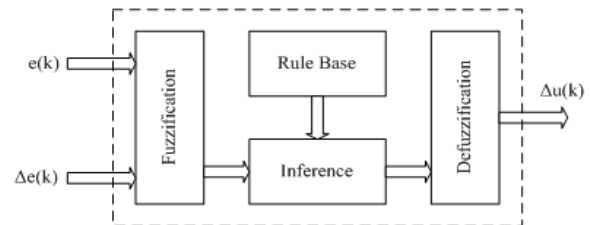

Fig.11.Fuzzy logic controller

The FLC involves three sections: fuzzification, impedance motor and defuzzification. The FC is described as I. seven fluffy sets for each info and yield. ii. Triangular enrollment capacities for straightforwardness. iii. Fuzzification utilizing ceaseless universe of talk. iv. Suggestion utilizing Madman's, 'min' administrator. v. Defuzzification utilizing the tallness technique.

Table III:Fuzzy Rules

e/Δe	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NM	NS	ZE	PS
NM	NB	NB	NB	NM	NS	PS	PM
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

Fuzzification: according to the Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The Partition of fluffy subsets and the state of enrollment CE(k) E(k) work adjust the get down to business to suitable framework. In this framework the information scaling factor has been outlined with the end goal that information esteems are between - 1 and +1. The info blunder for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}} \qquad (16)$$

$$CE(k) = E(k) - E(k-1) \qquad (17)$$

Inference Method: A few sythesis strategies, for example, Max– Min and Max-Dot have been proposed in the writing. In this paper Min strategy is utilized. The yield participation capacity of each administer is given by the base administrator and most extreme administrator. Table 1 indicates govern base of the FLC.

Defuzzification: As a plant more often than not requires a non-fluffy estimation of control, a defuzzification arranges is required. To figure the yield of the FLC, „height‟ technique is utilized and the FLC yield adjusts the control yield. Further, the yield of FLC controls the switch in the inverter.The set of FC rules are gotten from

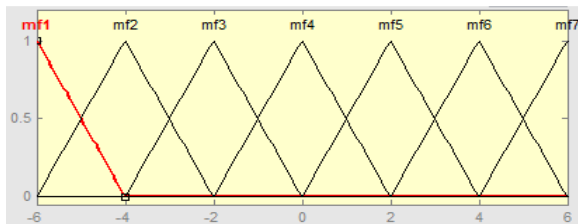$$u = -[\alpha E + (1-\alpha)*C] \qquad (14)$$

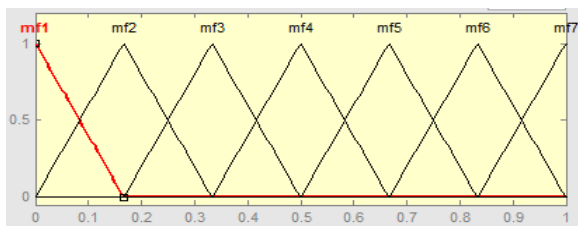Fig: 12 input error as membership functions

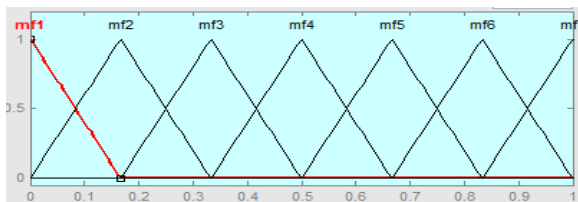Fig: 13 change as error membership functions

Fig: 14 output variable Membership functions

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.
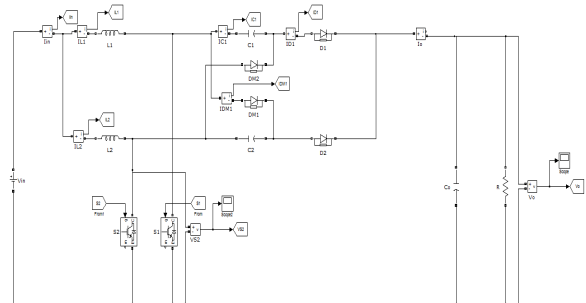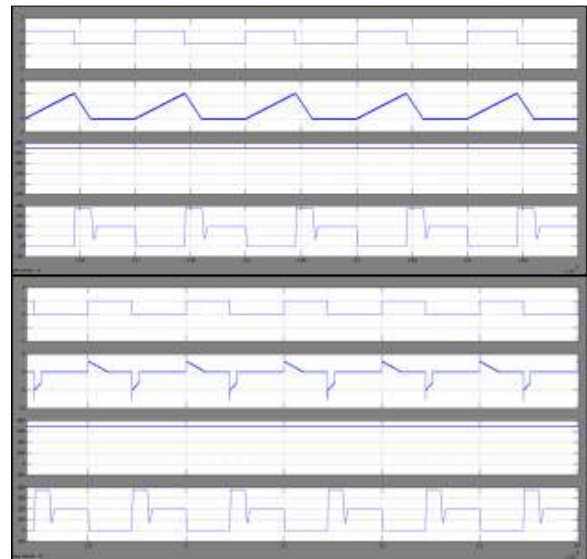
IX. Simulation Results

Fig :15Simulation block diagram of two-phase interleaved boost converter with voltage multiplier

A.   Static Simulations

The simulationalresults about at boundary condition are appeared in Fig. 16, which are as per the theoretical waveform in Fig. 4.
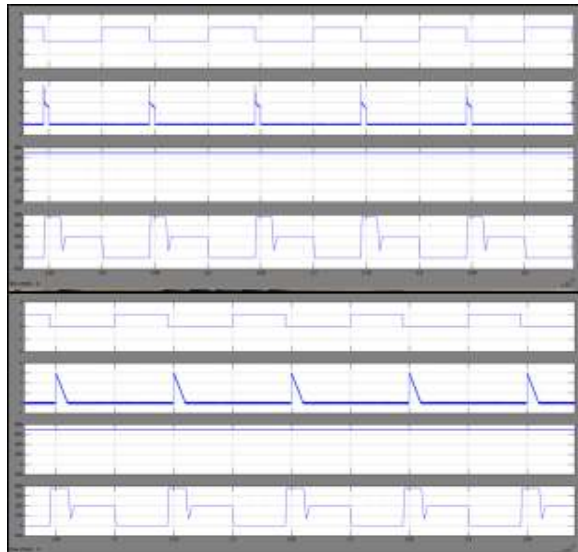
Fig. 18. Traditional interleaving control in Zone A (L = 1158 μH and R = 1658 Ω).

Fig. 16. Simulational results at boundary condition with traditional interleaving control (L = 1158 μH, R = 2023 Ω, and D = 0.448). (a) CH1-S1 Driver Voltage, CH2 − L1 Current, CH3-S1 Voltage Stress, CH4-Output Voltage, (b) CH1-S1 Driver Voltage, CH2 − C1 Current, CH3-S1 Voltage Stress, CH4- Output Voltage, (c) CH1-S1 Driver Voltage, CH2 − D1 Current, CH3-S1 Voltage Stress, CH4-Output Voltage, (d) CH1-S1 Driver Voltage, CH2 − DM 1 Current, CH3-S1 Voltage Stress, CH4-Output Voltage.

The reproduction comes about are given to confirm the past investigation. With R = 478 Ω, the output control is somewhat more prominent than 1 kW, and K = 0.048 >Kcrit = 0.011, the converter is intended to work in Zone A of Fig. 6(b), and the conventional interleaving control can keep up the voltage weight on switches with half of the yield voltage (i.e., 350 V) as appeared in Fig. 17.
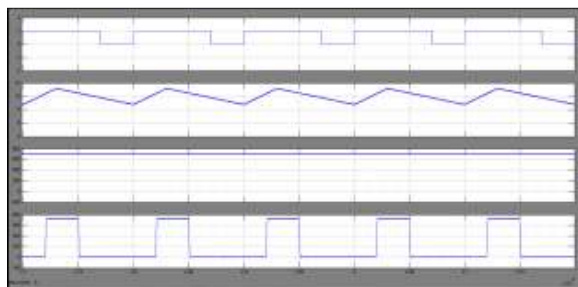
According to the comparison between the two control strategies are utilized and the outcomes which are appeared in Fig. 18 and Fig. 19, separately. In Fig. 19, traditional interleaving control is utilized, and we can see the voltage stress on the switch is 452 V which is higher than half of the output voltage.

Fig. 19. Traditional interleaving control in Zone B (L = 1158 μH and R = 3460 Ω).

Fig. 17. Traditional interleaving control at nominal load (L = 1158 μH and R = 478 Ω).

Therefore the R = 1658 Ω and K = 0.014 >Kcrit = 0.011, and the converter will continue operating in Zone A which is shown in the Fig. 6(b), along with the voltage stress on the power switches which is about 350 V which is represented as the half of its output which is shown in the Fig. 18.
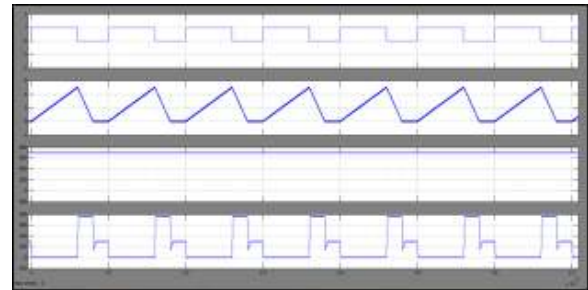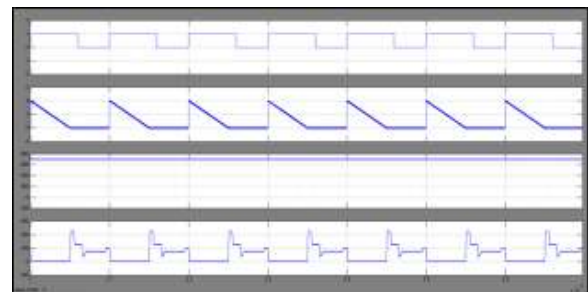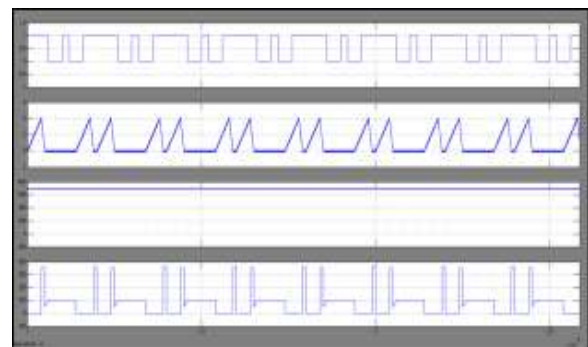

Fig. 20. APS control in Zone B (L = 1158 μH and R = 3460 Ω).

According to the Fig. 20, APS control is utilized, and we can see the voltage stress on the switch is 350 V which is about portion of the output voltage. Accordingly, it is compelling to utilize APS control when the converter works in Zone B. With the control technique as appeared in Fig. 8, more reenactments are directed to gauge the voltage weight on control switches in all power range of the load.

As appeared in Fig. 21, the voltage stress takes after the variety of the yield voltage, and nearly keeps half of the output voltage in all power value. The motivation behind why the output voltage isn't steady originates from the voltage swell of 20 V in the output voltage.
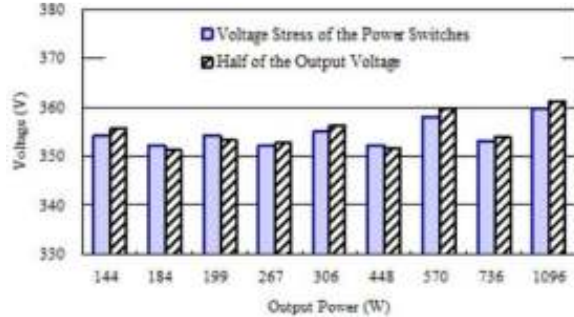

Fig. 22. Voltage stress on power switches in all power range of the load.
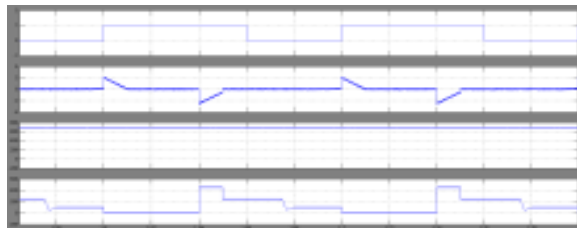

Fig. 23. Simulational results of current peak of capacitor C1 with traditional interleaving control under R = 3460 Ω.

According to the fig :23 the current with the capacitor will be 3.29A with the traditional interleaved control which is under the caries load R=3460 and the RMS value of current through the capacitor C1 is 0.623
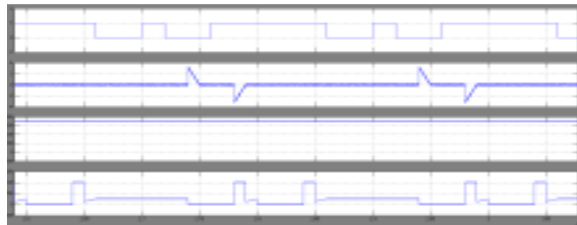

Fig. 24. Simulation results of current peak of capacitorC1 with APS control under R = 3460 Ω

According to the APS method when the current ripple will increases and it also decreases upto the 3.21A.under similar load which is shown in the fig :24 and also the RMS value of the current through the capacitor C1 which is decreases upto the 0.538A.
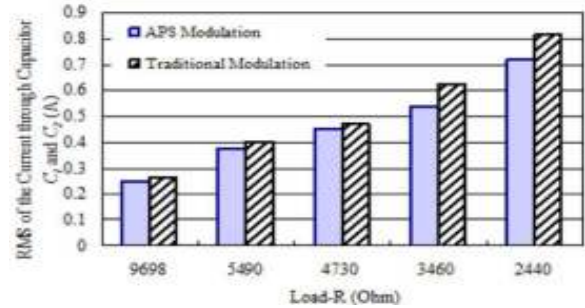

Fig. 25. Comparison on RMS of the current through capacitor (C1 and C2) with different control method below boundary condition (R > 2023 Ω).

According to the simulation which is conducted with the different load which is denoted in the Fig. 25, the current ripple with APS control which is less than the traditional interleaving control. In this way, the proposed APS control will increases the lifetime and capacitor C1 and C2.

The C1 and C2 are planned with film capacitor with the part number is SHB-500– 40– 4 from EACO Capacitor, Inc., and its most extreme RMS current is 19 A, which is considerably more prominent than the previously mentioned current ripple.

X. Conclusion

In this project we are analysis the boundary condition which has been derived. According to the boundary condition which have been classified into two cases such as zone A and zone B .in cases of zone A we are utilizing the traditional interleaving control and also according to the zone B we are utilizing the APS control. Therefore the swapping function while be achieved by the logic unit. According to the proposed control technique the converter can be achieved by the low voltage stress on the various switches in all the power range of the load and also by using fuzzy logic we can easy analysis the voltage stress and it will analysis like human brain which have been verified by the simulation results.

References

[1]   N. Sammes, Fuel Cell Technology: Reaching Towards Commercialization. London, U.K.: Springer-Verlag, 2006.

[2]   G. Fontes, C. Turpin, S. Astier, and T. A. Meynard, "Interactions between fuel cells and power converters: Influence of current harmonics on a fuel cell stack," IEEE Trans. Power Electron., vol. 22, no. 2, pp. 670–678, Mar. 2007.

[3]   P. Thounthong, B. Davat, S. Rael, and P. Sethakul, "Fuel starvation," IEEE Ind. Appl. Mag., vol. 15, no. 4, pp. 52–59, Jul./Aug. 2009.

[4]   S. Wang, Y. Kenarangui, and B. Fahimi, "Impact of boost converter switching frequency on optimal operation of fuel cell systems," in Proc. IEEE Vehicle Power Propulsion Conf., 2006, pp. 1–5.

[5]   S. K. Mazumder, R. K. Burra, and K. Acharya, "A ripple-mitigating and energy-efficient fuel cell power-conditioning system," IEEE Trans. Power Electron., vol. 22, no. 4, pp. 1437–1452, Jul. 2007.

[6]   B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/ switched-inductor structures for getting transformerless hybrid DC–DC PWM converters," IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 55, no. 2, pp. 687–696, Mar. 2008.

[7]   Z. Qun and F. C. Lee, "High-efficiency, high step-up DC–DC converters," IEEE Trans. Power Electron., vol. 18, no. 1, pp. 65–73, Jan. 2003.

[8]   H. Yi-Ping, C. Jiann-Fuh, L. Tsorng-Juu, and Y. Lung-Sheng, "A novel high step-up DC–DC converter for a microgrid system," IEEE Trans. Power Electron., vol. 26, no. 4, pp. 1127–1136, Apr. 2011.

[9]   L. Wuhua, F. Lingli, Z. Yi, H. Xiangning, X. Dewei, and W. Bin, "Highstep-up and high-efficiency fuel-cell power-generation system with activeclampflyback-forward converter," IEEE Trans. Ind. Electron., vol. 59, no. 1, pp. 599–610, Jan. 2012.

[10]   Y. Changwoo, K. Joongeun, and C. Sewan, "Multiphase DC–DC converters using a boost-half-bridge cell for high-voltage and high-power applications," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 381–388, Feb. 2011.

[11]   R. D. Middlebrook, "Transformerless DC-to-DC converters with large conversion ratios," IEEE Trans. Power Electron., vol. 3, no. 4, pp. 484– 488, Oct. 1988.