Indian J.Sci.Res. 17(2): 291-295, 2018 ISSN: 0976-2876 (Print)
ISSN: 2250-0138(Online)

FPGA HARDWARE IMPLEMENTATION OF A CORDIC-BASED RADIX-4 FFT PROCESSOR

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***Abstract*—**In this paper, the design of a CORDIC algorithm based radix-4 FFT processor is presented which is primarily intended to be used in power harmonic signal processing. The processor is implemented in a Field Programmable Gate Array (FPGA) that is characteristics of high efficiency, low cost, convenient implementation and short development cycle, and its performance is found to be satisfactory. The choice of the CORDIC algorithm for realizing the basic butterfly operation for the FFT which eliminates the need for storing twiddle factors and angles saves a lot of hardware compared to its counterparts employing other techniques. A dual-port memory structure and the corresponding addressing scheme are used to realize the inplace data access. The address generation unit required for fetching data from and writing results into the dual-port memory in proper sequence, is also incorporated within the chip which houses the controller as well. The full design is implemented using ALTERA CycloneII EP2C8Q208C8 series FPGA requiring approximately 3162 configurable logic blocks.

Keywords- CORDIC; Radix-4; FFT;FPGA

I. Introduction

With more and more non-linear devices used in the power grid, the contents of harmonics also increase, while the power quality has been required more strictly. Harmonics in power systems result in increased heating in the equipment and conductors, misfiring in variable speed drives, and torque pulsations in motors [1]. High levels of power system harmonics can create voltage distortion and power quality problems.

In order for the safe operation of power grids and power electronics technology to meet the needs of development, we must take effective measures to curb harmonics, and the harmonics test is first step of harmonic analysis.

At present, various approaches are available for harmonic detection. The method based on the instantaneous reactive power (IRP) theory, in which the harmonic signals are extracted from voltage and current measurements, has been widely utilized for harmonic compensation. But now it appears to need more researches suitable for digital control substituting for conventional analog control. As to the methods of wavelet transform [2] and neural networks [3] [4], only when each harmonic voltage and current amplitude and phase angle are worked out, can the harmonics content be found. Since the wavelet transform and neural network is so complex that they have not yet been widely used in practical projects. The most popular method of estimating harmonics in the power grids is still the method based on FFT, in which the magnitude and phase of each harmonics can be obtained. Because of a great deal of data processing, one has to use a high-performance technique, such as MCU and DSP [5] .But the clock frequency of MCU is limited, and it is difficult to satisfy the requirement of real-time. And also FFT processor designed with DSP, cannot easily update its function and expand its capacity that the customers need. Various ASIC FFT chips which are provided in high cost are restricted to widespread use.

FFT processor based on FPGA has widely used in signal processing, image processing and other fields. It has the characteristics with high parallel and throughput, and can meet some high real-time computing by using the FPGA device. Compared with conventional FFT processor by DSP or PC programming, it has a great advantage in speed. By using FPGA, not only the flexible configuration can be solved, but also the contradiction between the real time and accuracy in the detection of the power harmonics can be solved well.

In this paper, a new pipelined, reduced memory CORDIC based architecture is presented for a radix-4 FFT. A dual-port memory structure and the corresponding addressing scheme are used to realize in-place data accesses. The proposed memory-reduced CORDIC algorithm eliminates the need for storing twiddle factors and angles, resulting in significant area savings with no negative impact on performance. As a case study, the CORDIC-based Radix-4 FFT processor have been implemented in FPGA. The rest of this work is arranged as follows. In Section II, Radix-4 FFT and CORDIC algorithm fundamentals are briefly described. Then, the hardware architecture of the proposed CORDIC-based FFT is presented in Section III. The experimental results are provided in section IV and a look at future researches will be stated in the conclusion.

II. FFT AndCordic Algorithm

A. Radix-4 FFT Algorithm

The N-point discrete Fourier transform [6] is defined by

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$X(k) = \sum_{n=0}^{N-1} x(n)\, W_N^{nk}$, k = 0,1,….N-1

$W_N^{nk} = e^{-j2\pi nk/N}$ (1)

The radix-4 decimation-in-time FFT algorithm is described briefly in the following equations. The N-point input sequence is split into four subsequences, x(4m), x(4m+1),x(4m+2), x(4m+3), where k = 0, 1, ... , N/4-1.Thus DFT of the radix-4 decimation-in-time can be expressed as:

$$X(k)= \sum_{m=0}^{\frac{N}{4}-1} x(4m)\, W_N^{4mk} + \sum_{m=0}^{\frac{N}{4}-1} x(4m+1)\, W_N^{(4m+1)k} + \sum_{m=0}^{\frac{N}{4}-1} x(4m+2)\, W_N^{(4m+2)k} + \sum_{m=0}^{\frac{N}{4}-1} x(4m+3)\, W_N^{(4m+3)k} \quad (2)$$

Let $W_N^{4mk}=W_{\frac{N}{4}}^{mk}$, $W_N^k = W^p$,

$$A = \sum_{m=0}^{\frac{N}{4}-1} x(4m)\, W_N^{4mk},$$

$$B = \sum_{m=0}^{\frac{N}{4}-1} x(4m+1)\, W_{N/4}^{mk},$$

$$C = \sum_{m=0}^{\frac{N}{4}-1} x(4m+2)\, W_{N/4}^{mk} ,$$

$$D = \sum_{m=0}^{\frac{N}{4}-1} x(4m+3)\, W_{N/4}^{mk}$$

then Eq. (2) can be written as:

$X(k) = A + BW^p + CW^{2p} + DW^{3p}$

$X(k+N/4) = A - jBW^p - CW^{2p} + jDW^{3p}$

$X(k+2N/4) = A - BW^p + CW^{2p} - DW^{3p}$

$X(k+3N/4) = A + jBW^p - CW^{2p} - jDW^{3p}$ (3)

Eq.(3) can be expressed as Eq.(4) in a matrix form according to the characteristic of W_N^{nk}.

$$\begin{bmatrix} A' \\ B' \\ C' \\ D' \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -j & -1 & j \\ 1 & -1 & 1 & -1 \\ 1 & j & -1 & -j \end{bmatrix} \begin{bmatrix} A \\ BW^P \\ CW^{2P} \\ DW^{3P} \end{bmatrix} = Q \begin{bmatrix} A \\ BW^P \\ CW^{2P} \\ DW^{3P} \end{bmatrix} \quad (4)$$

Where

$A' = X(k)$, $B' = X(k+N/4)$, $C' = X(k+N/2)$, $D' = X(k+3N/4)$

Thus, a radix-4 butterfly computing unit can be viewed as the input sequences first multiplied by a rotating factor, then to a Q matrix left, which makes the total number of multiplications for the radix-4 FFT much less than that for the radix-2 FFT.

B. CORDIC algorithm

CORDIC algorithm was proposed by J.E.Volder [7]. It is an iterative algorithm to calculate the rotation of a vector by using only additions and shifts. Fig. 1 shows an example for rotation of a vector Vi. Equations (5) to (8) illustrate the steps for

calculating the rotation.

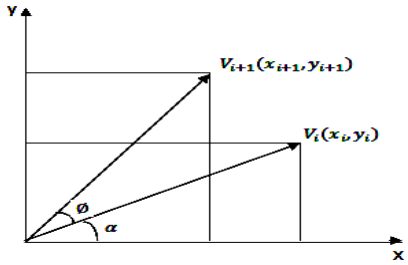

Fig.1 Schematic diagram of the transformation of $V_i(x_i, y_i)$to $V_{i+1}(x_{i+1}, y_{i+1})$

x_{i+1}= r cos($\alpha + \emptyset$)

= r(cos α cos ∅- sin α sin ∅)

=x_i cos ∅ - y_i sin ∅ (5)

y_{i+1}= r sin($\alpha + \emptyset$)

= r(sin α cos ∅-cos α sin ∅)

=y_i cos ∅ + x_i sin ∅ (6)

Let each rotation angle φ be equal to a r c ta n2^{-i}, then:

$x_{i+1} = \cos\emptyset(x_i - y_i \cdot 2^{-i})$ (7)

$y_{i+1} = \cos\emptyset(y_i + x_i \cdot 2^{-i})$ (8)

Since φ = arctan2^{-i}, cosφ can be simplified to a constant with fixed number of iterations:

$x_{i+1} = K_i(x_i - y_i \cdot d_i \cdot 2^{-i})$ (9)

$y_{i+1} = K_i(y_i + x_i \cdot d_i \cdot 2^{-i})$ (10)

Where $K_i = \cos(\arctan(2^{-i}))$and d_i= ±1 . Product of K_i's can be represented by the K factor which can be used as a single constant multiplication either at the beginning or end of the iterations. Then, (9) and (10) can be simplified as:

$x_{i+1} = (x_i - y_i \cdot d_i \cdot 2^{-i})$ (11)

$y_{i+1} = (y_i + x_i \cdot d_i \cdot 2^{-i})$ (12)

The direction of each rotation is defined by $d_i$and the sequence of all d_i's determines the final vector. $d_i$is given by:

$$d_i = \begin{cases} -1, & z_i < 0 \\ 1, & z_i \geq 0 \end{cases} \quad (13)$$

where$z_i$is called as angle accumulator and given by

$$z_{i+1} = z_i - d_i \cdot arctan\ 2^{-i} \qquad (14)$$

All operations described by Eqs.(11)-(14) can be implemented by only additions and shifts. Therefore, CORDIC algorithm does not require dedicated multipliers.

As shown in Eq.(1), the key operation of the FFT is $x(n) \cdot W_N^{nk}$, (where $W_N^{nk} = e^{-j2\pi nk/N}$ is just the so-called "twiddle factor"). This is equivalent to "Rotate x(n) by angle -$2\pi nk/N$ "operation which can be realized easily by the CORDICalgorithm. Without normal complex multiplication, CORDIC basedbutterfly can be very fast.

III. Proposed Cordic-Based FFT

A. The Overall Proposed FFT architecture

The overall structure of the proposed CORDIC-based FFT processor model is shown in Figure 2. The entire model is made of the address generation unit, the control unit, the dual port RAM unit, the 4-point butterfly unit and the CORDIC twiddle factor generation unit. This model is characterized by setting the parameter, sampling points and the accuracy to meet the actual needs. The FFT processor presented here is based on radix-4 DIT algorithm in which the in-place computation is utilized to achieve an efficient use of the memories. To perform these operations concurrently, a dual-port RAM has been employed. The control unit involves the timing control of the data storage, reading and writing to make the corresponding data and rotating factor coefficient flow into the butterfly and CORDIC computing unit in sequence in FFT operation. Data and addresses of the 'twiddle factor' can be easily generated by the counter. The address generation logic is very simple and does not limit the throughput of the system.

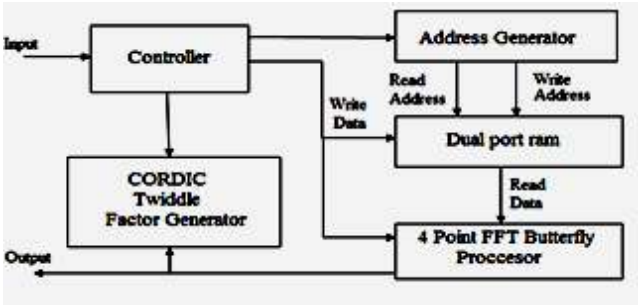

Fig.2 Proposed CORDIC-based FFT architecture

B. Module CORDIC

The CORDIC processor performs the vector rotation to compute a set of trigonometric functions. The principle idea of the CORDIC algorithm is to decompose a rotation into a sequence of micro-rotations. The pipelined CORDIC arithmetic unit can be obtained by decomposing the CORDIC algorithm into a sequence of operational stages[8].The corresponding stages are expressed by the following iterative Eqs. (11)-(14).

The CORDIC method can be employed in two different modes, known as the rotation mode and the vector mode. In this paper, one uses x and y to represent the real part and imaginary part of input and output vectors. In the rotation mode, the co-ordinate components of a vector and an angle of rotation are given and the co-ordinate components of the original vector are computed after rotation by a given angleIn the vector mode, the co-ordinate components of a vector are given and the magnitude and angular argument of the original vector are computed.

All the iterations of CORDIC algorithm are performed in parallel by using a pipelined structure [9], as shown in figure 3. The pipelined structure ensures the highest possible throughput, because a CORDIC transformation can be performed in each clock cycle.

C. FFT Butterfly Processor

Based on Eq.(4),four subsequences of FFT x(4m), x(4m+1), x(4m+2), x(4m+3) presented in the section II-A can be then schematized in Figure 4. The butterfly computation is the basic operator of an FFT processor. The operations of four complex additions and three complex multiplications need to be performed in each sequence of the radix-4 butterfly processor. Complex multiplication by twiddle factor can be replaced by the pipelined CORDIC algorithm. The complex multiplication is then transformed to CORDIC iterations in which only the adder and the shifter are used. In general, since the multiplication is much more expensive in term of computer operations than addition, the CORDIC method generally offer also considerable savings. In addition, the hardware consumption can be reduced significantly by using the CORDIC unit [10].

The output of each 4-point FFT is a linear combination of four signal sampling subsequences which are rotated and scaled by a K factor. This procedure will repeat $\log_4 N$times.

IV. Implementation Of 1024-Point FFT Processor And Experiment

The proposed design for the CORDIC-based radix-4 FFT processor has been realized by VHDL and implemented with an FPGA chip (Cyclone-II EP2C8Q208C8) on Quartus-II 9.1 platform.

With regard to the requirements of harmonic analyzer, the design and implementation of high-speed FFT processor is the most important work. Due to finite precision and the accuracy to meet the actual needs , the sampling points is 1024,which are processed in 5 stages by the FFT processor. The word length of the complex fixed-point data computed by butterfly processor is 16-bit. And the

CORDIC operator is implemented in a pipelined structure of 16 stages. The RTL synthesis view is shown in Figure 5.

Synthesis results shown in figure 6 confirm that the proposed design can reduce memory usage for FFT processors without amajor increase in the number of logic elements used. Furthermore, the implementation results and the post-simulation by ModelSim 6.5b are accordance with the theoretical analysis.

As shown in Figure 7, the system clock operates at 100MHz. The simulation results are as follows: it takes 51295ns to

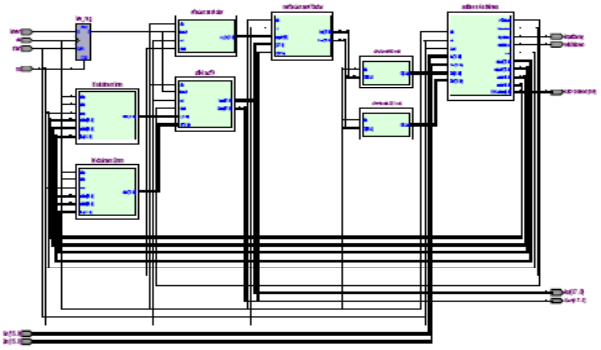

Fig.5 RTL of 1024-point FFT processor

Fitter Status	Successful - Sun Jan 09 01:38:05 2011
Quartus II Version	9.1 Build 222 10/21/2009 SJ Full Version
Revision Name	cfft1024X16
Top-level Entity Name	cfft1024X16
Family	Cyclone II
Device	EP2C88208C8
Timing Models	Final
Total logic elements	3,162 / 8,256 (38 %)
Total combinational functions	3,014 / 8,256 (37 %)
Dedicated logic registers	2,063 / 8,256 (25 %)
Total registers	2063
Total pins	104 / 138 (75 %)
Total virtual pins	0
Total memory bits	53,248 / 165,888 (32 %)
Embedded Multiplier 9-bit elements	0 / 36 (0 %)
Total PLLs	0 / 2 (0 %)

Fig.6 Synthesis results of 1024-point FFT processor

perform the operation of the system with a input signal in sine wave x= 5*sin(2*π *100*i/ Fs) of which Fs=1024 ,, and the output vectors of the real part are shown in yellow and the imaginary part in red. The blue wave is the spectrum computed by the output vectors between the real part and the imaginary part. The spectrum line distribution is accordance with the theoretical analysis at the position 100 and -100.

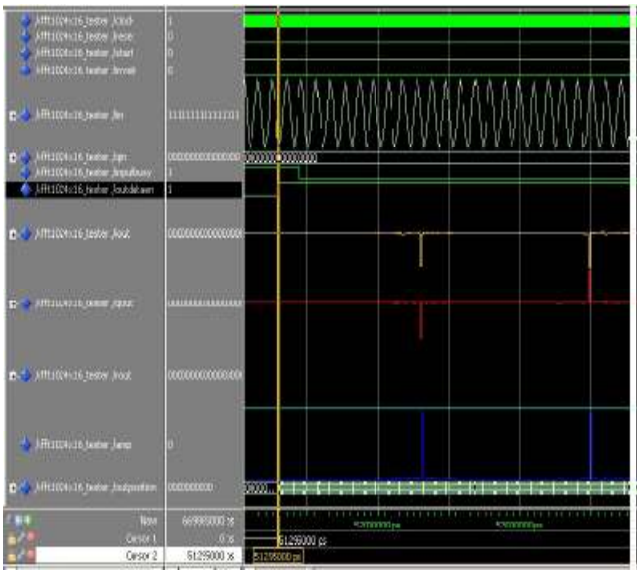

Fig.7 Modelsim simulation results of 1024-point FFT processor

V. Conclusion

In this paper, the design of a CORDIC algorithm based radix-4 FFT processor for spectrum analyzer using FPGA with its intended application in power harmonics signal processing is presented. The choice of the CORDIC algorithm for realizing the basic butterfly operation for the FFT which does not need storing twiddle factors and angles saves a lot of hardware compared to its counterparts employing other techniques. This kind of architecture can solve the contradiction between the real time and accuracy in the detection of the power harmonics well.

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