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INTRODUCTION TO REVERSIBLE SEQUENTIAL CIRCUITS

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Abstract - In this paper, the introduction of basic reversible logic gates are used for reversible operation and can be used for reversible sequential circuit design. When we say reversible computing, we mean performing computation in such a way that any previous state of the computation can always be reconstructed given a description of the current state. In recent years, reversible logic has many applications in quantum computing, low power CMOS optical computing and nanotechnology. This paper proposes a reversible D-latch and T flip-flop. We hope this paper will initiate a new area of research in the field of reversible sequential circuit.

Keywords - Reversible Logic, Reversible Logic Gate, D-latch, T Flip-Flop.

I. Introduction

Reduction of power dissipation remains one of the major goals in the VLSI circuit design for many years. R.Landauer demonstrated in early 1960s, that irreversible hardware computation results in energy dissipation due to the information loss, regardless of its realization technique [2]. It is proved that the loss of each one bit of information dissipates at least KTln2 joules of energy (heat), where K is the Boltzmann's constant and T is the absolute temperature at which operation is performed [2]. Reversible logic circuits have theoretically zero internal power dissipation since they do not lose information. Bennett showed that in order to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [3]. The applications of reversible logic are quantum computation [12], optical computing [13], ultra low power CMOS design [14] and nanotechnology [15].

This paper is organized as follows. Section II presents the basic definitions pertaining to reversible logic. Section III discusses the reversible logic gates. Section IV applications and Section V conclude/future work of the paper.

II. Basic Definitions Pertaining To Reversible Logic

A. Reversible Function

The multiple output Boolean function F(x1, x2,..., xn) of n Boolean variable is called reversible if:

1. The number of outputs is equal to the number of inputs.
2. Any output pattern has a unique pre-image.

In other words, the reversible functions are those that perform permutations of the set of input vectors.

B. Reversible Logic Gate

A reversible gate is a logical cell that has the N number of inputs and N number of outputs with a one-to-one mapping between the input and output vector. For the logical cell to be reversible the following two conditions are not permitted.

1. Direct fan-outs from the reversible gates.
2. Feedback from a gate output directly to its input.

The block diagram of irreversible XOR gate and reversible XOR gate is as shown in fig 1.

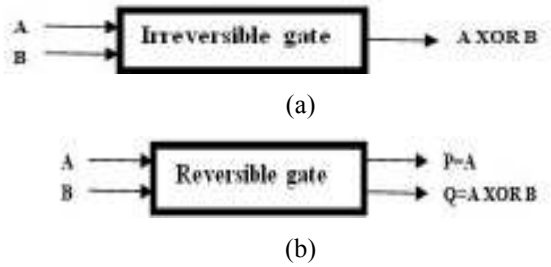

Fig 1: (a) Irreversible XOR gate (b) Reversible XOR gate

C. The number of Reversible gates (N)

This refers to the number of reversible gates used in circuit.

D. The number of constant inputs (CI)

This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.

E. The number of garbage outputs (GO)

This refers to the number of unused outputs present in a reversible circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.

F. Quantum cost (QC)

This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated by knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

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G. Flexibility

This refers to the universality of a reversible logic gate in realizing more functions.

H. Gate Level

This refers to the number of levels in the circuit which are required to realize the given logic functions.

I. Hardware Complexity

This refers to the total number of logic operation in a circuit. Means the total number of AND, OR and EXOR operation in a circuit.

J. Design constraints for Reversible Logic circuits

In the design of any reversible logic circuits the following points must be considered to achieve an optimized circuit.

- Fan-out is not permitted.
- Minimum quantum cost.
- Garbage outputs must be minimum.
- Constant inputs must be minimum.
- Minimum number of logic depth or gate levels.
- Minimum delay.

III. Reversible Logic Gates

A reversible logic gate has equal number of input and output terminals and there is one to one mapping between them. Again we can say, gate is reversible if we can determine input vector from output vector and vice-versa. Reversible gate should practically loose very little amount of energy. Fan-out is not allowed in reversible circuits however fan-out can be achieved using additional gates. In this paper we have discussed basic reversible gates like Feynman gate, Fredkin gate, Toffoli gate, Peres gate and Sayem gate. Which we have used in implementing reversible sequential circuits.

A. Feynman Gate

Feynman gate is a 2*2 one through reversible gate as shown in figure 2. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A XOR B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate [19].

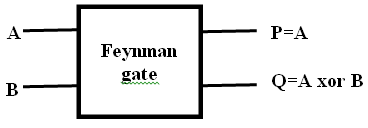

Fig 2: Feynman gate

B. Toffoli Gate

Fig 3 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are given by P=A, Q=B, R=AB XOR C. Quantum cost of a Toffoli gate is 5[5].

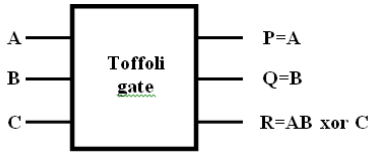

Fig 3: Toffoli gate

C. Fredkin Gate

Fig 4 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=AC XOR A′B and R=AB XOR A′C. Quantum cost of a Fredkin gate is 5[6].

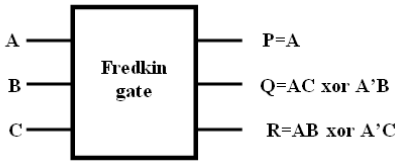

Fig 4: Fredkin gate

D. Peres Gate

Fig 5 shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A XOR B and R=AB XOR C. Quantum cost of a Peres gate is 4[20].

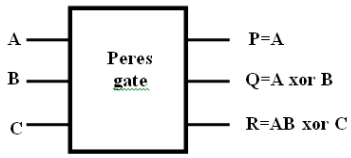

Fig 5: Peres gate

E. Sayem Gate

Fig 6 shows 4x4 sayem gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). The output is defined by P=A, Q=A'B XOR AC, R=A'B XOR AC XOR D, S=AB XOR A'C XOR D [10].

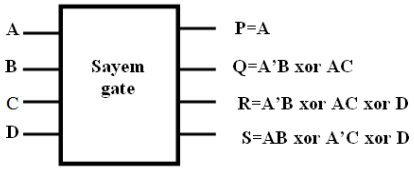

Fig 6: Sayem gate

F. Latches

Here we can use D-Latch or T-Latch depending upon choice that can be used in implementing reversible sequential circuit (counter) [21].

1. D-Latch

The characteristic equation of D-Latch is Q^+=DE+E'Q. It can be realized with one SG. It can be mapped with SG by giving E, Q, D and 0 respectively in 1st, 2nd, 3rd and 4th input of SG. Fig 7 shows the design of D-Latch with only Q output and Fig 8 shows the design of reversible D-Latch with both the output Q and Q+ .One FG is needed to copy and produce the complement of Q from SG for the design of Fig 7(b) [24].

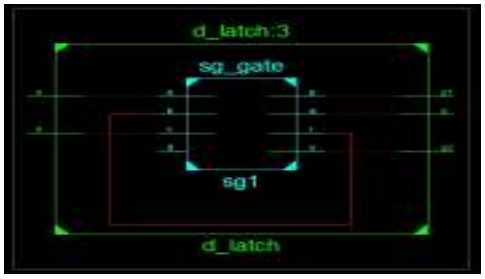

Fig 7: Design of D-Latch with only output Q

Fig 8: results of D-Latch with only output Q

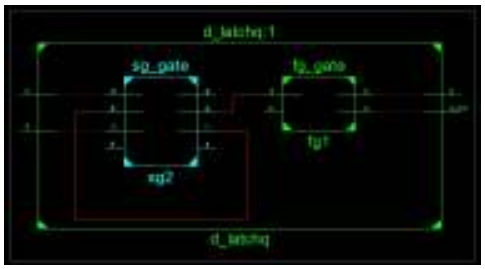

Fig 9: Design of D-Latch with output Q and Q^+

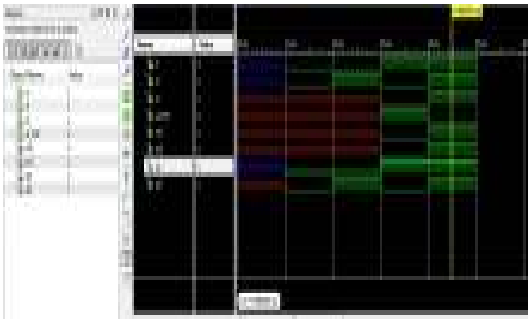

Fig 10: results of D-Latch with output Q and Q+

2. T-Flip Flop

As the name suggests, this flip-flop circuit used to toggle the output when input is high (1) and retains the output when input is low (0), thus it does two operation, it either holds the last state or toggles the output. Essentially, it has a logical symmetry with Controlled NOT kind operation.

T	Q_{t+1}
0	Q_t
1	Q_t^+

Table I: Truth table of T flip-flop

The reversible realization of T Flip-flop has two SG gates and one Feynman Gate is shown in fig 8 [22].

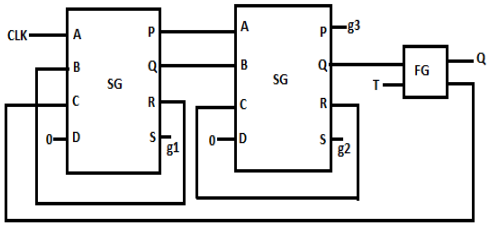

Fig 11: Reversible Positive Edge Triggered T flip-flop

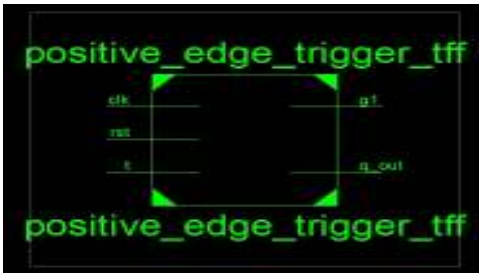

Fig 12: Reversible Positive Edge Triggered T flip-flop

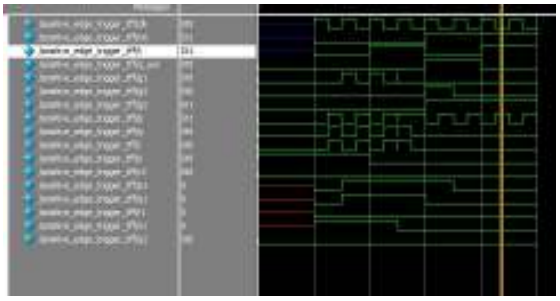

Fig 13: Results of Reversible Positive Edge Triggered T flip-flop

IV. Applications

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

- Low power CMOS.
- Quantum computer.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.
- Design of low power arithmetic and data path for digital signal processing (DSP).
- Field Programmable Gate Arrays (FPGAs) in CMOS technology.

V. Conlusion And Future Scope

This paper proposes designs of basic reversible sequential elements such as latches, flip-flop.

The proposed sequential circuit designs have the applications in reversible ALU, reversible processor etc.

This work forms an important move in building large and complex reversible sequential circuits for quantum computers. The future work could be to develop efficient reversible counters and reversible controller circuits.

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