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ANALYSIS AND DESIGN OF SINGLE PRECISION FLOATING POINT MULTIPLIER USING PERES RLG

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***Abstract*—** The proposed concept describes an design analysis of an IEEE 754 single precision floating point multiplier using Peres RLG targeted for Xilinx Virtex-4 FPGA. Reversible logic concept is used to reduce the power consumption as compared to classical logic and it also reduces losses occurred during information bit access. So many computation techniques can adopt the reversible logic concept such as low power computing, quantum computing, optical computing, and other emerging computing technologies. Peres gate is one of the simple reversible logic gate and its quantum cost is 4. Because of its simplicity as well as lowest quantum cost, Peres gate is used to design entire single precision floating point multiplier circuit. Verilog is used to implement a technology-independent pipelined design. The proposed design can be made to handle overflow and underflow cases. Rounding is not implemented to give more precision when using the multiplier in a Multiply and Accumulate (MAC) unit. Rounding may also be implemented by truncation method for further reduction in power and area. The entire design is modelled using Verilog hardware description language .The coding is done on Xilinx ISE 12.2 and simulation is performed on Modelsim 6.3.

***Keywords*—** Floating point; RLG; FPGA; Quantum computing; MAC; Truncation; MFLOPs.

I. Introduction

Reversible logic concept will become more popular in the recent years because of their ability to reduce the power dissipation or power consumption. The main requirement in low power VLSI design is low power dissipation so reversible logic concept has wide range of applications in low power CMOS and Optical data processing, DNA computing in medical field, quantum cost computation and so on. In Irreversible or classical hardware computation energy dissipation due to information loss will occurs. So Landauer's research, states that the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where K is the Boltzmann's constant and T is the temperature at which operation is performed. The heat generated (energy dissipated) due to one bit information loss is very small at room temperature but when the number of bits is more as in the case of high speed computation application the heat dissipated or energy dissipated by them will be so large that it affects the performance and it reduces the lifetime of the components used in the circuit. In 1973, Bennett showed that KTln2 energy would not dissipate from a system if system allows process of reproduction of inputs from observed outputs. Reversible logic concept also has an ability to run the system in both forward and backward direction. So the reversible logic computations can generate inputs from outputs and vice-versa. A circuit is said to be reversible if its input vectors can be uniquely recovered from its output vectors and there is a one-to-one correspondence called one-to-one mapping between its input and output assignments, so inputs can be recovered from outputs similarly outputs can also recovered from its inputs. In such way the energy dissipation can be reduced or even eliminated by performing the lossless information computation.

Any reversible logic gate has same number of input and output vectors. If a reversible logic gate has k inputs, and then obviously it has k outputs, then we call it as a k x k reversible logic gate. The additional outputs added in order to make the number of inputs and outputs equal but they are not actually used in the synthesis of a given function. Sometimes such outputs mandatorily used to achieve reversibility property such additional outputs are called as garbage.

Floating point numbers are the one possible way of representing real numbers in binary format. The IEEE 754 standard presents two different types of floating point formats, one is Binary interchange format and Decimal interchange format is other type. Multiplication of floating point numbers is a critical issue in DSP applications. So the proposed paper focuses only on single precision normalized binary interchange format. Figure 1 shows the representation of IEEE 754 single precision binary format. The format consists of an one bit sign (S), an eight bits of exponent (E), and a Twenty three bits of fraction (M or Mantissa). An extra bit is added to the fraction to form the significand. The condition is that if the exponent is greater than zero and smaller than 255, and there is 1 in the MSB bit of the significand then the number is said to be a normalized, in such case the real number is represented by (1)

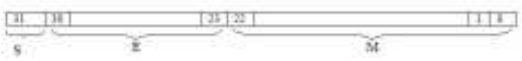

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Fig.1 IEEE single precision floating point format

$$Z = (-1^{s}) * 2^{(E - Bias)} * (1.M)$$

Where $M = m_{22}\,2^{-1} + m_{21}\,2^{-2} + m_{20}\,2^{-3} + \ldots + m_{1}\,2^{-22} + m_{0}\,2^{-23}$

Bias = 127

To multiply two numbers in floating point format is done by 3 important steps:

- Addition of exponent of the two numbers then subtracting the bias from added result.
- Next step is to multiply the significand of the two numbers.
- Finally calculate the sign by XORing the sign of the two numbers. In order to represent the multiplication result as a normalized number the condition is that, there should be 1 in the MSB of the result (leading one).

II. Proposed Contributions

A number of works have been reported in the literature with an aim to achieve a reduced latency of floating –point operations. Survey on different techniques as well as components is systematically reported bellow.

Landauer [1] determined that the amount of energy dissipated or heat generated to erase each bit of information is at least kTln2 (where k is the Boltzmann constant i.e. $3x10^{12}$ joule at room temperature) during any computation the intermediate bits used to compute the final result are erased this is the main reason for the power dissipation. Therefore amount of power depends on number of intermediate bits used.

C. H. Bennett [2] in 1973 proposed that the power dissipation or heat generation in any device can be made zero or less if the computation is done using reversible logic model. Also he proved a theory with the help of the Turing machine which is a symbolic model for computation introduced by Turing. Bennett also showed that the computations that are performed by the irreversible or classical machine can perform with same efficiency on the reversible machine. By considering all the concepts mentioned above the research on the reversibility was started in the year of 1980.

In the year 1994 Shor [3] proposed his remarkable research work in creating an algorithm using reversibility for factorizing larger number with better efficiency when compared to the classical or irreversible computing theory. After this the work on reversible computing was started by more people in different fields such as emerging technologies like nanotechnology, quantum computers and low power CMOS VLSI and so on.

Based on the concept of reversibility Edward Fredkin and Tommaso Toffoli [4, 5] introduced new reversible logic gates known as Fredkin and Toffoli reversible logic gates. These gates have zero energy dissipation and also they are used as universal gates in the reversible logic based circuits. These gates have three input and three outputs, hence they known as 3x3 reversible logic gates.

Peres [6] also invented a new gate known as pares gate. Peres gate is also a 3x3 gate but it is not a universal logic gate like Fredkin and Toffoli logic gates. Even though this gate is not universal gate it is widely used in many application because it has less quantum cost when compared to the universal logic gates. The quantum cost of the Peres gate is four. H Thapliyal and N Ranganathan [7] also invented a reversible gate known as TR gate. The major objective of invention of this reversible logic gate was to reduce the garbage output in a reversible logic based circuits.

The main objective of invention of IEEE-754 standard for Floating Point Arithmetic [8], intended for hardware implementation, although provisions were made for software implementation for other operations. In addition to required operations, an appendix of recommended functions was also specified. Default exception handling capability was specified, and provisions for alternate exception handling capability were also provided. Lacking in the standard means to access many of the features from higher level languages as well. Because of the standardization it is possible to write algorithms using floating point arithmetic which could be executed on a variety of platforms and which would produce identical results. Also it became possible to prove statements regarding the behaviour of floating point programs. In 2000, the IEEE chartered a new committee to examine the IEEE-754 standard with the goals of including a decimal floating point arithmetic, incorporating good existing practice, providing for reproducible results, and clarifying the standard, while not invalidating conforming implementations of the IEEE-754(1985) standard.

The concept proposed by Mohamed Al-Ashrafy, Ashraf Salem, and Wagdy Anis [10] describes an efficient implementation of an IEEE 754 single precision floating point multiplier. The multiplier implementation handles the over/under flow cases. To achieve more precision rounding is not implemented when using the multiplier in a multiply and Accumulate (MAC) unit. In some (truncated) multiplication technique by truncation method rounding may also be implemented for further reduction in power and area. With latency of three clock cycles the design achieves 301 MFLOPs.

In the recent years due to low power dissipation reversible logic has emerged as a promising technology having its wide range applications in many fields like low power CMOS, quantum computing, nanotechnology, and optical computing. The classical or irreversible set of gates such as AND, OR and XOR are not reversible. Recently a 4 x 4 reversible logic gate called "TSG" is proposed by Himanshu Thapliyal and M.B Srinivas [11]. The most significant aspect of the proposed reversible logic gate is that it can perform singly as a reversible full adder, that is reversible full adder can now be implemented with a single gate only. The proposed design is NXN reversible multiplier using TSG gate. It is based on two concepts. The partial products can be generated in parallel with a delay of d using Fredkin reversible gates and thereafter the addition can be reduced to log2N steps by using reversible parallel adder designed from TSG logic gates. Similar multiplier architecture in conventional arithmetic (using conventional logic) has been reported in existing literature, but the proposed one is totally based on reversible logic and reversible cells as its building block. TSG gate is much better and optimized, compared to its existing counterparts in literature, in terms of number of reversible gates and garbage outputs.

Field programmable gate arrays (FPGA) are popularly used in the high performance and scientific computing community to implement floating-point based system. In the year 2012 M.Jenath, V.Nagarajan [13], proposed the reversible single precision floating point multiplier (RSPFPM) it requires the design of reversible integer multiplier (24X24) based on operand decomposition approach. Reversible logic is used to reduce the power dissipation compared to classical logic and do not allows the information loss which finds application in low power computations, quantum computing technology, optical computing, and other emerging complex computing technologies. Among the reversible logic gates, Peres gate is utilized to design the multiplier because of its lowest quantum cost.

In 2014 Madivalappa Talakal [14] proposed REA using peres gate. The most significant aspect is that REA using peres gate can gives lowest quantum cost as well as garbage output.

In 2014 April [15] he also made the brief survey on reversible logic technique as well as single precision floating point multiplier using reversible logic.

In 2014 May Madivalappa Talakal [16] again proposed 8X8 reversible multiplier using Peres gates. The most significant aspect is that 8X8 reversible multiplier using Peres gate can gives lowest quantum cost as well as garbage output.

III. Concept Of Reversible Logic

A reversible logic gate is a k-input- k-output logic device with one-to-one mapping property. This helps to determine the outputs from the inputs and vice-versa (reproducibility). Also in reversible circuits synthesis direct fan-Out is not allowed that is one–to-many concept is not reversible. However implementation of fan-out in reversible circuits is achieved by using additional gates. Reversible logic circuits should be designed using less number of reversible logic gates as much as possible. From the point of reversible logic circuit design, there are many parameters for determining the performance and complexity of circuits. Some of them are given bellow.

- The number of Reversible gates utilized (N): The number of reversible gates used in circuit.
- The number of constant inputs used (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to realize or synthesize the given logical function.
- The number of garbage outputs used (GO): This means the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are much essential to achieve reversibility property.
- Quantum cost of designed circuit (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate in it. The quantum cost calculation helps for knowing the number of primitive reversible logic gates (1x1 or 2x2) required to realize the circuit.

The important design constraints for reversible logic circuits are given bellow.

- Reversible logic gates do not allow fan-outs (one to many).
- Reversible logic circuits should maintain minimum quantum cost.
- To produce minimum number of garbage outputs the design can be optimized so the reversible logic circuits must use less number of constant inputs.
- The reversible logic circuits must use a minimum logic depth (reduced complexity) or gate levels.

A. Reversible Logic Gates

Power dissipation is important factors in low power VLSI design. The recent computers for every time erase a bit of information and dissipate the power in terms of heat while they perform a logical operation. Such logical operations are called "irreversible logic"(classical logic). An example of information loss can be seen in an ordinary NAND gate. ANAND gate has two inputs and only one output, which means we loss one bit of information in the process of moving from the input to the output of the gate.

Such drawbacks are overcome by reversible logic concept. Main advantages of reversible logic are low power consumption, due to the reduction in the information loss, so automatically it minimizes the power dissipation. Reversible logic gate is a k x k logic device with one-to-one mapping property. This is used to determine the outputs from the inputs and also the inputs can also be recovered from the outputs. Figure 2(a) and 2(b) shows the classical gate (irreversible gate) and general NXN reversible gate. In the reversible XOR gate there is no information loss will occurs. Since it maps the input vector with output vector which gives the equal number of inputs and outputs.

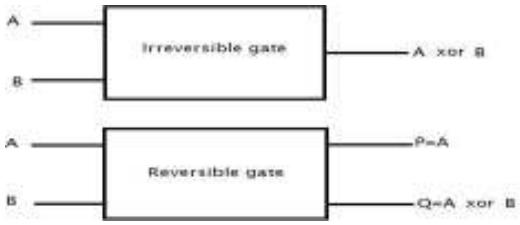

Fig .2 (a) Irreversible XOR Gate (b) Reversible XOR Gate

The simplest reversible logic gate is basic NOT gate and is 1x1 reversible gate. Controlled NOT (CNOT) gate is another type of 2x2 reversible gate. There are many 3x3 reversible logic gates exist they are Fredkin gate, Toffoli gate, Peres gate and TR gate. The cost associated with each reversible logic gate is called as quantum cost. The quantum cost of 1x1 reversible gates is 0, and quantum cost of 2x2 reversible gates is 1. Any reversible logic gate is realized by using 1x1reversible NOT gates and 2x2 reversible gates, such as V and V+ (V is square root of NOT gate and V+ is hermitian of NOT gate) and Feynman gate which is also known as controlled NOT gate (CNOT).following sections.

The property of V and V+ quantum gates is given bellow

V x V = NOT

V x V+ = V+ x V = I

V+ x V+ = NOT

Except few cases quantum cost of a reversible gate can be calculated by counting the number V, V+ and CNOT gates used in implementing it.

B. Not Gate

This is the only reversible gate among the conventional logic gates. This is also called as 1x1reversible logic gate with quantum cost of 0.

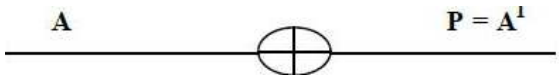

Fig.3 Not gate

C. Feynman Gate

Feynman gate is a 2x2 reversible logic gate as shown in figure

4. The input vector is I = (A, B) and the output vector is O = (P, Q). The outputs are defined as P=A, Q=A xor B. Quantum cost of a Feynman gate is one.

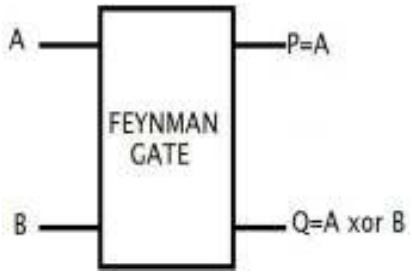

Fig.4 2X2 Feynman gate

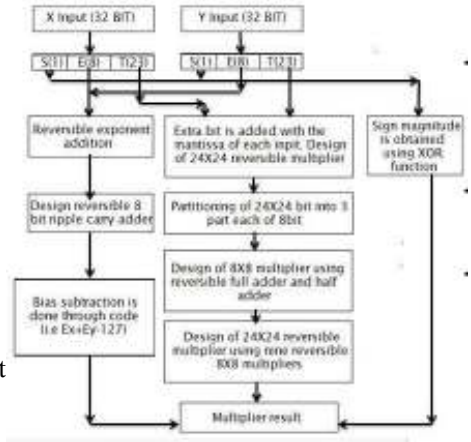

Fig.6 Block diagram of RSPFPM

a)Sign Bit Calculation

The XOR function of X and Y gives the proper sign of multiplied product. The XOR function is implemented in the design by using single Peres gate.

D. Peres Gate

Figure 5 shows a 3x3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output is P = A, Q = A xor B and R=AB xor C. Quantum cost for Peres gate is 4. In many designs Peres gate is used because of its lowest quantum cost.

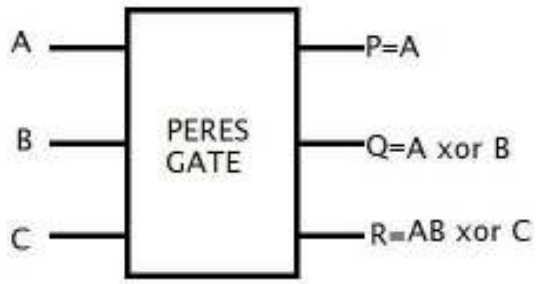

Fig.5 3x3 Peres gate

IV. Proposed Methodology

The figure 6 represents the block diagram of reversible single precision floating point multiplier (RSPFPM). Peres gate is used to design entire structure is modelled using Verilog code. The coding is done on Xilinx ISE 12.2 for simulation purpose the Model sim 6.3 has been used. So the detailed explanation

A. Exponent Adder

The exponents are added by using 8X8 reversible ripple carry adder and the bias value -127 is subtracted from exponents result. The basic building block in the ripple carry adder is full adder, and most other adder circuits. So in this proposed paper single Peres gate is used to design half adder and using 2 half adders the necessary full adder is designed. So Peres gate is basic building block of proposed design and it has an ability to perform all necessary operations. The full adder has 3 inputs X_i, Y_i and C_i and computes the sum bit S_i and carry bit C_{i+1}. The equations for sum and carry output bits are given bellow.

$$Sum_i = X_i \oplus Y_i \oplus C_i \quad (2)$$

$$C_{i+1} = X_i Y_i + X_i C_i + Y_i C_i \quad (3)$$

Reversible ripple carry adder An 8-bit reversible ripple carry adder is used to add the two input exponents. As shown in Figure 7, a ripple carry adder is a chain of cascaded full adders and one half adder. Each full adder has 3 inputs (A, B, C_i) and 2 outputs (S, C_o). The carry out (C_o) of each adder is fed to the next full adder (ripple the carry from previous stage to next).

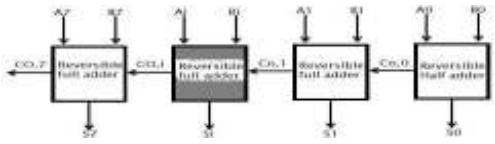

Fig.7 Reversible Ripple Carry adder

The addition process produces an 8 bit sum (S7 to S0) and a carry bit (Co, 7). Bias is subtracted from 9 bit addition result (S8 to S0). To minimize the circuit complexity as well as area required the operation of Bias subtraction is directly obtained from the Verilog code; this eliminates the use of subtractor. So in this way total efficiency of final system will increases in terms of amount of power required as well as number of reversible logic gates (peres) used.

B. Reversible Multiplier

The multiplier portion in the above figure 6 is a reversible 24X24 multiplier and to reduce the complexity initially it is divided into 3-8X8 reversible multipliers. An 8x8 bit unsigned multiplication is performed in a reversible manner by utilizing only the Peres gate for the design to generate the 64 one bit partial products. Simple 8X8 multiplier operation is shown in figure 8. The Figure 5 shows the quantum cost of Peres gate. The 64 partial products are obtained for 8x8 bit reversible multiplication $X \times Y = ([x7, x6, \ldots x0 \quad y7, y6, \ldots y0])$ and

is shown in figure 9. Peres gate provide the necessary AND operator when their input C is hardwired to 0 and also Peres gates reduces the quantum cost. In the summation stage of multiplier Peres gate is used because a cascade of two Peres gate can generate the full adder operation. This design realizes a lower quantum cost and fewer garbage outputs by virtue of proposed design of reversible full adder and half adder. So the entire multiplier part designed and implemented using Verilog code. The coding is done on Xilinx ISE 12.2 for simulation purpose the Model sim 6.3 has been used.

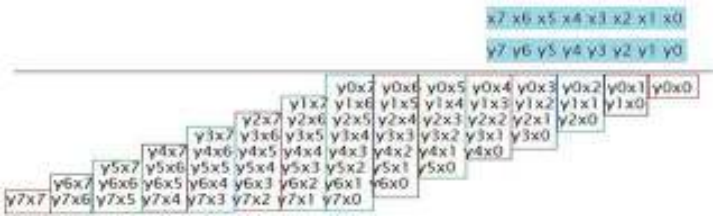

Fig.8 16 bit output in the reversible 8X8 multiplier

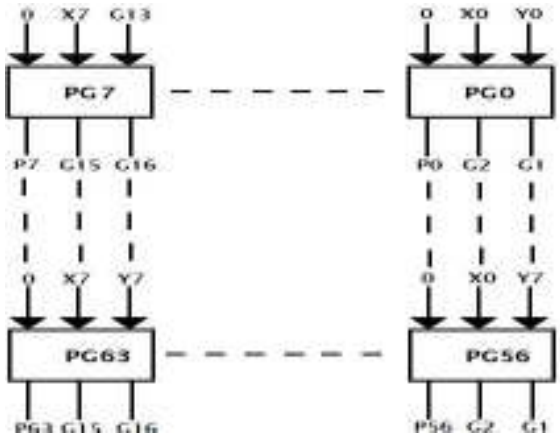

Fig.9 Generation of 64 partial products

V. Simulation And Results

The entire design of single precision floating point multiplier using reversible logic is modelled using (Verilog) HDL .The Xilinx ISE 12.2 is used for coding. The Modelsim 6.3is used for simulation purpose. The simulation result for proposed multiplier is shown in Figure 11. Finally the proposed multiplier will be efficient in terms of number of reversible gates and garbage output. Reduction in number of gates reduces the complexity of circuit. Table.1device utilization summary confirms that the proposed design uses very few slices (165), LUTs (288) and bonded IOBs (128).

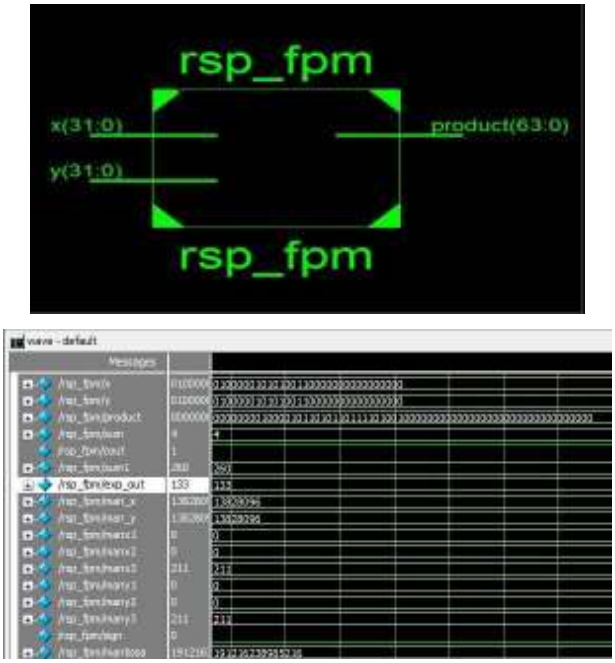

Fig.11 Simulation result of RSPFPM

Table I. Device Utilization Summary

Logic utilization	Used	Available	Utilization
Number of slices	165	5472	3%
Number of 4 input LUTs	288	10944	2%
Number of bonded IOBs	128	320	40%

VI. Applications

Because of low power dissipation reversible concept has wide range of applications some of them are given bellow:

- Low power CMOS VLSI design.
- Quantum computers.
- Nanotechnology and microelectronics.
- Optical computation.
- Design of efficient low power arithmetic for digital signal processing systems (DSP).

VII. Conclusion

This paper presents a design analysis of a single precision floating point multiplier using Peres reversible logic gate supports the IEEE 754 binary interchange format. Basic reversible gates presented in this paper can be used in regular circuits realizing Boolean functions. The reversible exponent addition using reversible ripple carry adder, 8X8 reversible multiplier and sign bit generator are designed by using peres gate and modelled by Verilog hardware description language. The proposed multiplier uses such parts to accomplish its reversible multiplication operation and is efficient in terms of number of reversible gates and garbage output and also in terms of quantum cost. Reduction in number of gates to reduce complexity of circuit. Finally by observing table.1 it confirms that the proposed design uses very few slices (165), LUTs

(288) and bonded IOBs (128). Reversible computing may have long-term benefit very well in those areas which require high energy efficiency, speed and performance. In future the proposed work may be implemented by using different reversible logic gates in order to improve the performance compared to proposed one.

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