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A DESIGN ON LOW- POWER ADDER OPERATING ON EFFECTIVE DYNAMIC DATA RANGES

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***Abstract*—**To design a power-efficient digital signal processor, this study develops a fundamental arithmetic unit of a low-power adder that operates on effective dynamic data ranges. Before performing an addition operation, the effective dynamic ranges of two input data are determined. Based on a larger effective dynamic range, only selected functional blocks of the adder are activated to generate the desired result while the input bits of the unused functional blocks remain in their previous states. The added result is then recovered to match the required word length. Using this approach to reduce switching operations of noneffective bits allows input data in 2's complement and sign magnitude representations to have similar switching activities. This investigation thus proposes a 2's complement adder with two master-stage and slave-stage flip-flops, a dynamic-range determination unit and a sign-extension unit, owing to the easy implementation of addition and subtraction in such a system. Furthermore, this adder has a minimum number of transistors addressed by carry-in bits and thus is designed to reduce the power consumption of its unused functional blocks. The dynamic range and sign-extension units are explored in detail to minimize their circuit area and power consumption. Experimental results demonstrate that the proposed 32-bit adder can reduce power dissipation of conventional low-power adders for practical multimedia applications. Besides the ripple adder, the proposed approach can be utilized in other adder cells, such as carry look ahead and carry-select adders, to compromise complexity, speed and power consumption for application- specific integrated circuits and digital signal processors

Keywords -Low-power design, number-representation, switching activity, dynamic range, digital

I. Introduction

BREAKTHROUGHS in low-power technologies are extending running times for portable devices employing media processing and communication applications . To accomplish these applications, many researchers have proposed advanced low-power techniques at the algorithm level, system level, architecture level, circuit design level, and fabrication process level. The algorithm of a specified application can be modified to compromise algorithmic performances with computational complexity. At the system level, active, idle and sleep operational modes can be achieved by managing clock frequency signals. Meanwhile, hardware designs utilize parallel and pipeline schemes to reduce power consumption by lowering supply voltage. The power saving capabilities of circuitry incorporating low-power circuit diagrams and of manufacturing processes that use silicon on insulator and reduced threshold voltages are well known. Three major sources of power dissipation in digital CMOS circuits are switching, short circuits, and leakage. Particularly, the switching activity at capacitive nodes is a major source of power dissipation. This switching power can be illustrated by the following:

$$P_{switching} = \infty C V_{dd}^2 f_{clk}$$

Where∞denotes the switching activity factor, C represents the loading capacitance,Vdd is a supply voltage and ***fclk***is the operating frequency. Herein, can be interpreted as the effective loading capacitance of switching operations. According to (1), several approaches can reduce switching power. First, the supply voltage can be reduced, since switching power is proportional to the square of the supply voltage. However, this approach extends the circuitry delay. Second, the operational frequency can be reduced, but this also reduces the throughput rate for the system application. Third, the switching activity of an effective loading capacitance can be minimized via various algorithmic, architectural, logic, and circuit techniques; however, doing so may increase circuit area or delays. Additionally, efficiently numerically representing a digital system is essential to reducing switching power. Generally, the 2's complement representation for arithmetic operations involving addition and subtraction is easy to implement in a hardware design. However, due to sign extension, an arithmetic operation for small dynamic ranges of input data may require switching power throughout the entire word length. One means of minimizing switching activities in sign-extension bits is to use sign-magnitude representation, in which a single bit is allocated for the sign while the remainder of the bits are allocated for the magnitude. In such a case, if the dynamic range of a datum does not span the entire word length, only one bit toggles when the datum switches sign. Sign-magnitude representation can effectively reduce the number of transitions on busses, but requires a complicated architecture to conduct addition and subtraction operations

The evolution of portable or mobile communication devices such as laptops, cellular phones, video games, etc. is the most important factor driving the need for low power design. The main reason behind the development of low power circuits is that many portable devices and their applications require low power dissipation and high throughput. The commercial

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success of portable or mobile devices depends significantly on their weight, cost, and battery life. In most cases, the cost and weight of batteries become a bottleneck that prevents the reduction of system cost and weight. Moreover, for most portable systems, the IC (Integrated Circuit) components consume a significant portion of the total system power. Portable devices have a strict demand for power consumption since they have limited battery capacity. Low power design also plays a significant role in high-performance integrated circuits such as microprocessors and other high-speed digital circuits. Due to the increase in clock frequency, there is a proportional increase in power dissipation. The power consumed by the integrated circuit is dissipated in the form of heat. This may lead to problems such as circuit degradation and operating failures. The power consumption in microprocessors is projected to grow linearly in proportion to their die size and clock frequency. Various cooling systems have been introduced to reduce the heat from power dissipation and keep the chip temperature at an admissible level. This in turn has increased the packaging cost, which results in large revenue.

The switching power of an arithmetic unit originates from the bit switching activities of two input data changing from x(n- 1) and y (n-1) to x(n) and y(n) respectively. Looking at each input datum, it can be partitioned into effective and noneffective bits according to its effective dynamic range. Switching activities between the bits of x(n-1) and the corresponding bits of x(n) can thus have four cases of switching from effective to effective (EE) bits, from effective to noneffective (EN) bits, from noneffective to effective (NE) bits and from noneffective to noneffective (NN) bits. The four patterns above have switching activities in the 2's complement representation. The switching activities of the sign magnitude and hybrid number representations follow the EE, EN and NE cases. Meanwhile, no switching activity occurs for the NN case in the sign magnitude representation due to a lack of sign-extension bits.

This study thus develops a 2's complement adder with two master-stage and slave-stage flip-flops, a dynamic-range determination unit and a sign-extension unit to reduce power consumption . Depending on the effective dynamic data range, the functional blocks of an adder are only partially activated to perform their operations. Furthermore, the unused functional blocks consume less switching power because they are fed with unchanged input bits. After summation, the final result is reconstructed to match the original word length by using sign extension. The ripple adder with the minimum number of transistors addressed by carry-in bits is especially realized in hardware implementation. Meanwhile, the dynamic-range determination and sign-extension units are designed to minimize circuit area and power consumption.

II. The Proposed Arithmetic Operations

Addition is a fundamental arithmetic operation in which input data can be represented by different numerical representations. The two most widespread numerical representations are 2's complement and sign magnitude. Fig.(1)displays an illustrative example of switching activities in effective and noneffective bits. Two 16-bit data of x(n) and y(n) in the 2's complement representation are added together where x(n-1) and y(n-1) are zero. The most significant 8 bits of x(n) and y(n) are all 0 and 1, respectively, that are noneffective bits. The summation result(n) reveals its most significant 8 bits becoming zero. This effect shows that an adder for computing sign-extension bits contains numerous switching activities. In such a case, if an 8-bit adder is used rather than a 16-bit adder, power consumption can be significantly reduced. Therefore, this study exploits the feasibility of dynamically allocating the functional blocks of an adder to various dynamic data ranges. Power could then be saved from the unused functional blocks of the adder.

$$
\begin{array}{rl}
x(n) & 0000\ 0000\ 0110\ 0010 \\
+\ y(n) & 1111\ 1111\ 1110\ 0111 \\
\hline
z(n) & 0000\ 0000\ 0100\ 1001
\end{array}
$$

Fig. 1.A 2's complement addition.

The proposed addition operation, as shown in Fig.(2)Can be realized in the 2's complement and sign magnitude representations. Before performing an addition operation, the effective dynamic ranges of the two input data are determined. With a larger effective dynamic range, only some of the functional blocks of an adder are activated to perform addition. The added result is then scaled to match the original word length according to its numerical representation. The unused functional blocks consume minimal switching power because their input bits remain in the previous states.

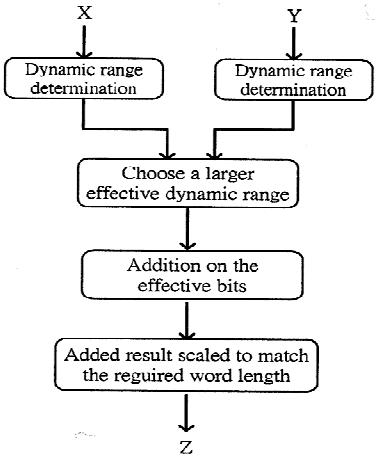

Fig. 2.The proposed addition operation.

III. The Proposed Low-Power Adder

The data flows of a 2's complement addition operation in the conventional and proposed approaches

are shown in Fig. (3).According to the conventional data flow, illustrated in Fig. 3(a),input data are latched by flip-flops and then pipelined into a summation unit. To reduce power consumption, the proposed data flow, as displayed in Fig. 3(b), includes input data latched in master-stage flip-flops, dynamic-range determination, effective bits latched in slave-stage flip-flops, data summation, and sign extension. The dynamic-range determination (DRD) unit located between the master-stage and slave-stage flip-flops determines the effective dynamic range of the input data stored in the master-stage flip-flops. Control signals are then generated to enable the paths for the effective bits to be stored in the slave-stage flip-flops. Such a design enables bit switching in slave-stage flip-flops to be reduced through effective dynamic data ranges. Additionally,to save power only some of the functional blocks of an adder are activated to perform an addition operation in small dynamic data ranges, because the other functional blocks have unchanged input bit values. After summation, the outcome is recovered to have the original word length by using a sign-extension (SE) unit that copies the value of a sign bit to the most significant unused bits. The proposed low-power adder includes two master-stage flip-flops, a dynamic-range determination unit, two slave-stage flip-flops, a ripple adder, and a sign-extension unit. These functional units are described below.

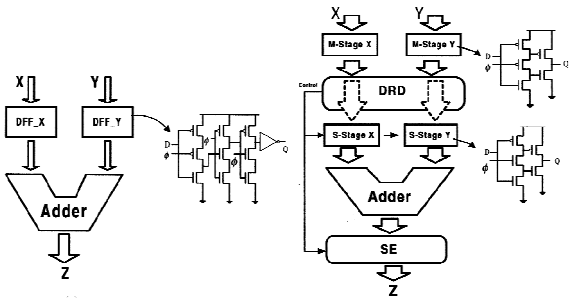

Fig.3. Data flows of a 2's complement addition operation. (a) A conventional data flow and a typical flip-flop design. (b) The proposed data flow, and typical master-stage and slave-stage flip-flop designs.

A. Master-Stage and Slave-Stage Flip-Flops

The master-stage and slave-stage flip-flops, shown in Fig. 3can be built using true-single-phase edge-triggered circuitry that provides high-speed and power-efficient pipeline operations.

B. Dynamic-Range Determination Unit

The dynamic-range determination unit detects the larger effective dynamic range from the two input data. Control signals are then generated with this dynamic range to manipulate slave-stage flip-flops and the sign-extension unit. The dynamic range detection can be realized by using groups of bits to simplify the hardware implementation. For example, a 32-bit datum with a dynamic data range of 32, 28, 24, 20, 16, 12, 8, or 4 bits can be determined if group detection is based on 4 bits. The number of bits of a basic group is represented by Ndrd. .A 32-bit datum can be partitioned into 8 groups, from G7 to G0 , each having four bits. The 5-bit comparator must be employed to check the continuous four bits of Gi and the most significant bit of Gi-1. If these 5 bits are all either 0 or 1, an active control signal, Pre ctl, is generated. An additional bit in the neighbouring group is considered to ensure continuous comparison, and to move the sign bit to the most significant bit of the group with effective bits. Fig. (4) hows the functional blocks of the dynamic-range determination unit, which includes comparators and NOR gates for Ndrd equal to 4. Herein, a 32-bit adder has two input data, each requiring 7 comparators to determine its effective dynamic range. Fig. 5(a) shows an –bit comparator for the case where Ndrd equals n-1.This comparator that only includes the pass transistors, dynamic pull-up and pull-down transistors and an XOR gate can be easily scaled to any high-bit one at low-complexity and low-power manners. The larger effective dynamic range of the two input data is determined by using the NOR operations on the Pre ctl signals from the comparators. Fig. 5(b) shows a low-power pre-discharged multiple-input NOR gate for the number of input bits larger than 4.

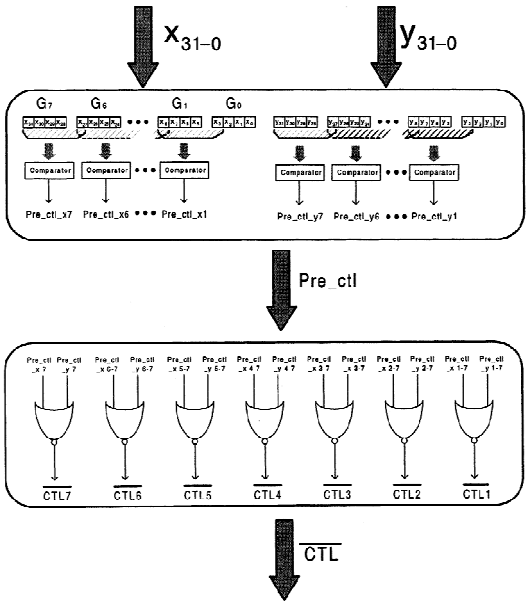

Fig. 4 The dynamic-range determination unit for Ndrd equal to 4.

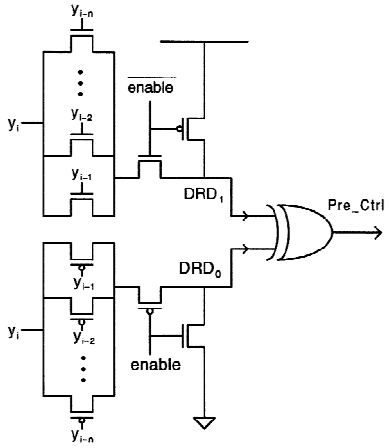

Fig (a)

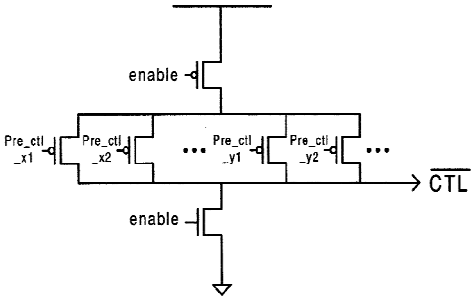

Fig (b)

Fig. 5 Functional units of the dynamic-range determination unit. (a) An-bit comparator. (b) A multiple-input NOR gate

C. An Adder

In the proposed approach, the adder can be constructed with ripple, carry-skip, carry-select, carry lookahead circuits, and so on . This study aims mainly to reduce the switching activities of functional units for noneffective bits. The conventional adder did not control the carry bit between the used and unused functional blocks of an adder. If this carry bit has a switch, the unused blocks whose input bits remain in previous states contain little switching power. Implementing a ripple adder based on a 1-bit addition unit with four transistors addressed by a carry bit, as shown in Fig. 6.an reduce this switching power.

D. Sign-Extension Unit

After an adder is operated, the results in the effective and noneffective dynamic ranges will be correct and incorrect, respectively. Hence, the sign bit in the effective dynamic range needs to be copied to the most significant bits in the noneffective dynamic range. Fig.7displays the functional blocks of the sign-extension unit when Ndrd equals 4. The control signals from the NOR gates of the dynamic-range determination unit are latched by the additional slave-stage flip-flops that synchronize the addition and sign-extension operations. These control signals, CTL and $\overline{CTL}$, are decoded by a sign-selection function to generate signals, S-ctl , for telling pass transistors to select a correct sign value. Additionally, CTL manipulates the multiplexers that pass the added results and the sign-extension value. By using the proposed sign-extension unit, a result that matches the original word length is recovered.

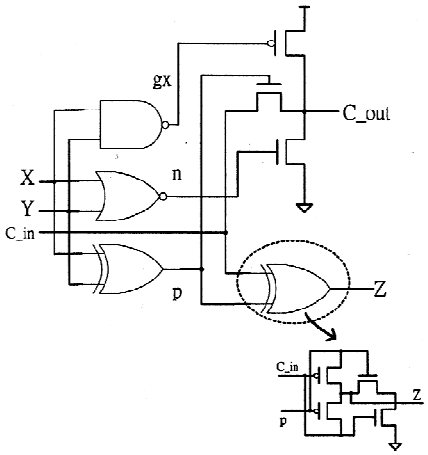

Fig. 6.A 1-bit adder with four transistors addressed by a carry-in

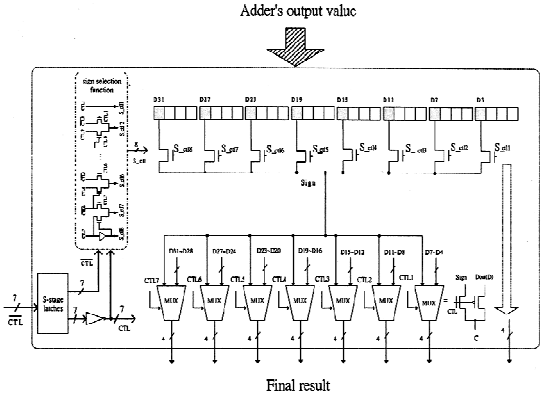

Fig. 7. The sign-extension unit for N drd equal to 4.

IV. Power Analyses And Comparisons Of The Proposed And Conventional Adder

The proposed low-power adder includes two master-stage flip-flops, a dynamic-range determination unit, two slave-stage flip-flops, a 32-bit ripple adder, and a sign-extension unit. The adder is designed to reduce the power consumption of the dynamic-range determination and sign-extension units. Fig. 8 shows the average power of the conventional adder, and proposed adder in of 1, 2, 4, and 8, when the effective dynamic ranges of 32-bit input data have uniform distributions ranging from to and bits. The average power of the proposed adder is smaller than that of the conventional adder when exceeds 2. Restated, the average power of

dynamic-range determination and sign-extension units is less than the switching power of functional units for noneffective bits, implying that the proposed adder can save power.

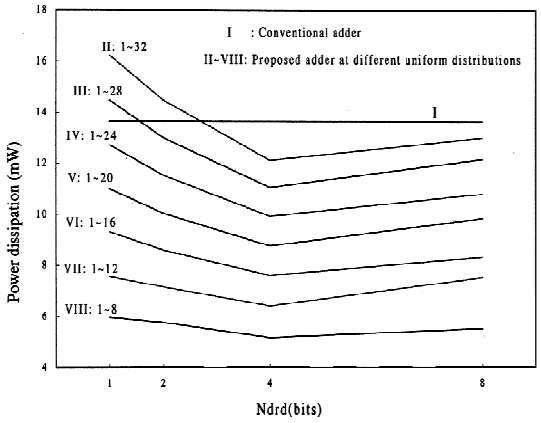

Fig. 8. Average power of the proposed 32-bit adder in Ndrd of 1, 2, 4, and 8 for effective dynamic ranges of input data with uniform distributions from 1 to 8; 12; . . . ; and 32 bits.

V. Conclusion

This study has successfully developed a low-power addition operation that dynamically partitions an adder into used and unused functional blocks according to the effective dynamic ranges of the input data. Switching of noneffective bits are minimized in our 2's complement addition operation. The proposed 32-bit adder, with two master-stage and slave-stage flip-flops, a dynamic-range determination unit and a sign-extension unit, is well designed and is analysed according to effective dynamic ranges of input data with the uniform and Gaussian distributions. Additionally, an adder with a minimum number of transistors addressed by carry-in bits is designed to reduce power consumption of unused functional blocks. The dynamic range determination and sign-extension units are effectively designed to minimize power consumption. This study also presents several practical examples of image, video, and audio applications using both the proposed and conventional adders. Simulation results demonstrate that the proposed adder can employ dynamic-range determination and sign-extension units to trace the dynamic ranges of input data and hence conduct computations more power-efficiently than conventional adders. As well as the ripple adder, the proposed approach can be utilized in the carry lookahead and carry-select adders to compromise complexity, speed and power consumption. Therefore, the proposed adder can be widely used in ASIC and DSP for power-efficient computing in multimedia applications.

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